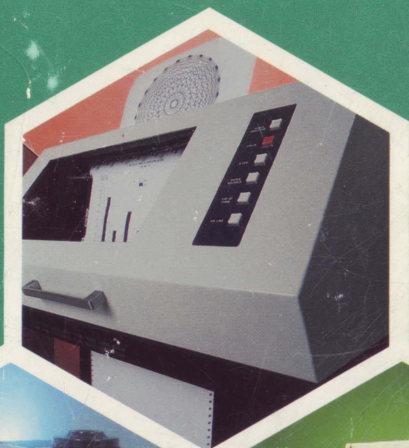
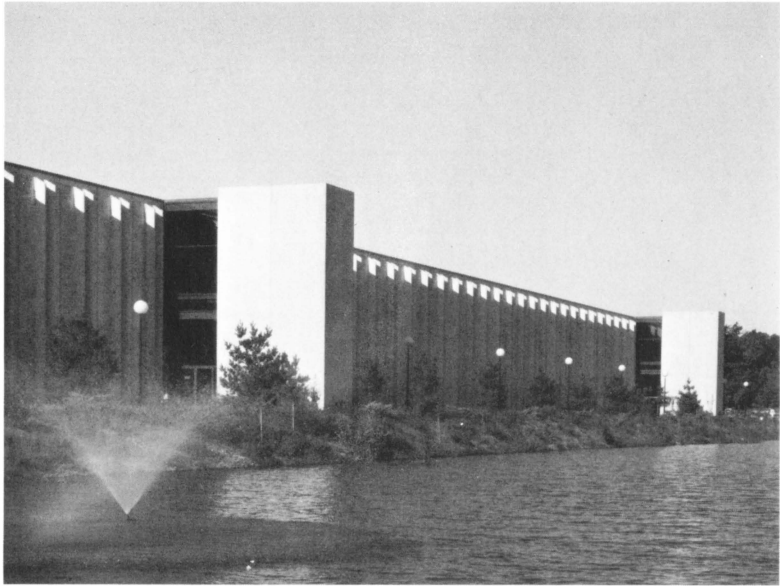


# peripherals handbook



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*DIGITAL Facility, Parker Street, Maynard, Massachusetts*

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# CHAPTER 1

## INTRODUCTION

DIGITAL's family of computer peripherals is continually growing to provide you with the hardware that most precisely meets your needs. Cost effectiveness, capacity, ease of use, reliability, maintainability, and serviceability are constantly being upgraded.

The two most recent additions to DIGITAL's family of computer peripherals supported by VAX systems are the RP07 disk drive, utilizing Winchester fixed-media technology, and the TU78 magnetic tape transport, using Group Coded Recording (GCR) technology. These new peripherals combine state-of-the-art microprocessor control, large capacity, high speed, and self-test diagnostics. Other new disk drives include the RM80 and RM05. The RM80 disk drive, which also utilizes Winchester fixed-media technology and advanced microprocessor control, is supported on VAX systems. The RM05 is supported on both VAX-11/780 and PDP-11/70 systems. The latest lineprinters include the high-speed LP11-E band lineprinter with 64- and 96-character sets and the high-speed LXY21 printer/plotter, both supported by UNIBUS PDP-11 systems and VAX systems.

With the purchase of one of DIGITAL's peripherals, you will receive detailed user and maintenance documentation. This information may be supplemented by the excellent tutorial guides to DIGITAL's software languages and operating systems and by other volumes in the Handbook series. DIGITAL's Educational Services group offers a wide range of hardware and software courses specifically designed to address customers' needs.

In addition, DIGITAL's Computer Special Systems (CSS) group provides customers with design service and products to complement the corporation's high volume offerings. CSS products address the customers' needs in the process I/O, graphics, networks products, and special terminals marketplaces.

The Peripherals Handbook contains chapters on all of DIGITAL's currently-marketed UNIBUS PDP-11 and VAX disks, magnetic tapes, lineprinters, card readers, and sensor I/O devices. It should be used in conjunction with the Terminals and Communications Handbook which describes DIGITAL's terminals and communications equipment.

This book is divided into chapters by device type. Each chapter is further subdivided into sections by device. Each section contains the following:

- an introduction
- a list of features
- a general description
- packaging information
- data formats and data organization information (where applicable)
- operation description
- interrupt information
- reliability/maintainability features
- controls and indicators (where applicable)
- specifications

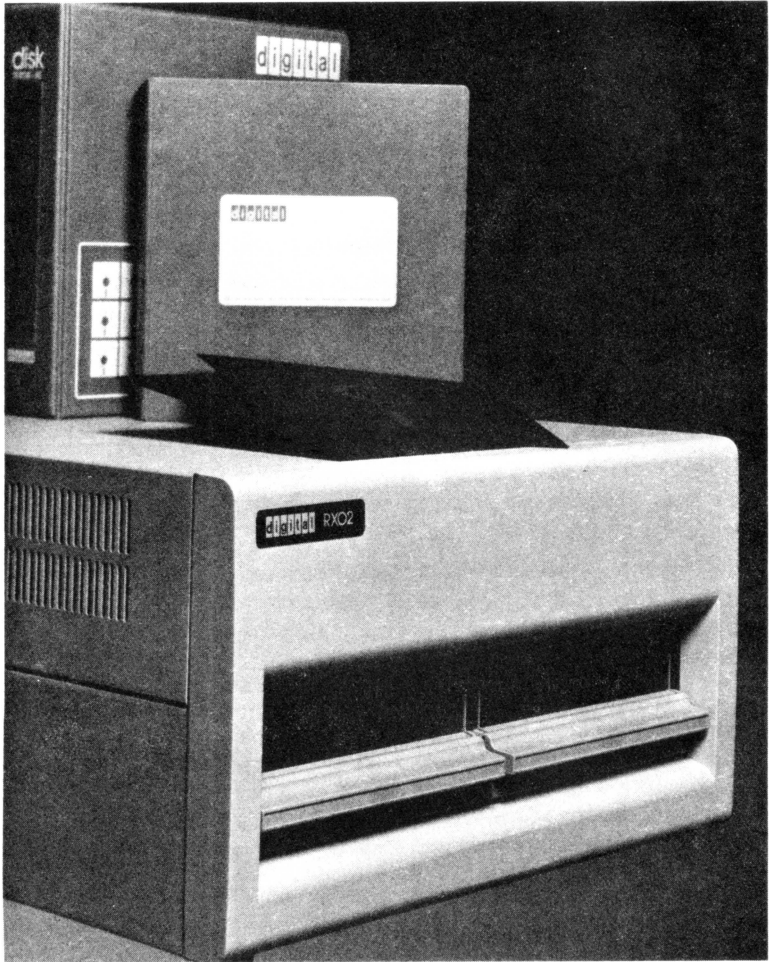
At the end of the disk, magnetic tape, lineprinter, and card reader chapters is a comparison chart of the peripherals in that chapter. This allows easy comparison among like devices to ensure the best selection for your needs. The specification information is subject to change without notice, and should be considered as a guide only. For specific site preparation information, please consult your local DIGITAL sales office.

Chapter 7 contains the register diagrams and bit definitions for all the peripherals described in this book. The appendices contain additional, relevant information including an ASCII code chart, a standard and compressed Hollerith code chart, and UNIBUS addresses and vector assignments for DIGITAL'S peripherals.

In addition to the Peripherals Handbook, DIGITAL's series of handbooks includes the Terminals and Communications Handbook, the PDP-11 Processor and Software Handbooks, the Microcomputer Processor, Microcomputer Interfaces, and Microcomputers and Memories Handbooks, and the VAX Hardware, Software, and Architecture Handbooks.







**RX211**

## CHAPTER 2

# DISK DRIVES

### **RX211**

The RX211 is a dual-drive, double density, floppy disk subsystem connected to the UNIBUS via an interface/controller. The RX211-BA(BD) subsystems are supported by UNIBUS PDP-11 systems. VAX-11/750 systems also support the RX211-BA(BD) subsystems, but only as a data file resident device for transport of data to and from other DIGITAL systems. The low cost of the RX211 subsystem makes it ideal for archive storage, diagnostic loading, or software updates.

### **FEATURES**

- Double density recording provides greater data storage capacity
- Program-selectable single density mode provides compatibility with other floppy disk subsystems
- 0.5 MB of formatted data storage capacity per diskette (1 MB total per RX211 subsystem)
- Direct Memory Access (DMA) data transfers
- Microprocessor controller
- Compact, removable diskettes

### **DESCRIPTION**

The RX211-BA(BB) floppy disk subsystems consist of two RX02 floppy disk drives, a microprocessor controller, an interface/controller, and a 15 ft (4.6 m) I/O cable. Up to two RX211 subsystems (a total of four RX02 floppy disk drives) are supported by UNIBUS PDP-11 systems and VAX-11/750 systems.

The RX211 floppy disk subsystems use industry standard diskettes. They are thin, flexible disks similar in size to a 45-rpm phonograph record. These diskettes are recorded on one side only. In double density mode, each diskette can store 0.5 MB of data. The program-selectable single density mode provides compatibility with other floppy disk subsystems, such as the RX11.

### **RECORDING METHODS**

The RX211 reads/writes data in two modes: single density, which utilizes frequency modulation (FM) recording, and double density, which utilizes modified frequency modulation (MFM) recording. The RX211 normally reads/writes data in double density mode. Single density mode can be read or written by the RX211 subsystem to provide



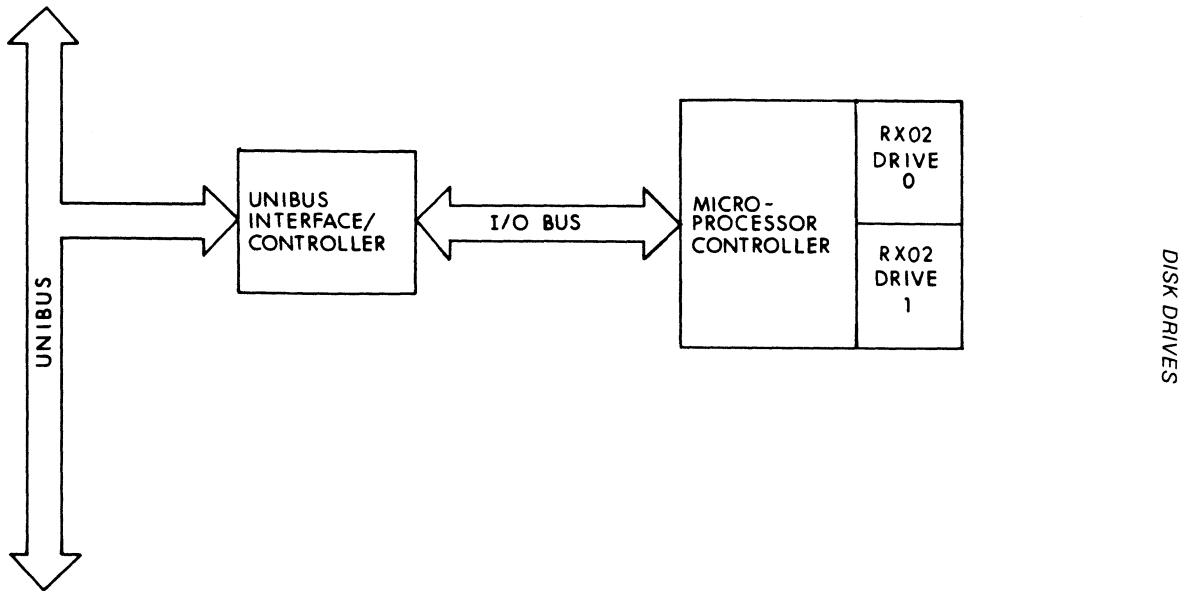


Figure 2-1 RX211 SYSTEM BLOCK DIAGRAM

compatibility with other floppy disk subsystems. Data is written on the diskette by magnetizing small sections (bit cells) of the oxide on the diskette in different directions, i.e. either positively or negatively. A change in the direction of magnetization (flux transition) in the clock area or data area of a bit cell indicates whether the bit represented is a 1 or a 0.

### **DATA ORGANIZATION**

The RX211 has one read/write head that is used to both read and write data. The diskette surface is divided into 77 tracks. Each track is divided into 26 sectors with a data storage capacity of 2048 bits (256 bytes). Each sector is divided into a header field and a data field. The header field consists of a header preamble, a 56-bit header that contains the track and sector addresses, and a 16-bit header CRC (Cyclic Redundancy Check). The data field consists of a data preamble, an 8-bit code specifying the recording density, 2048 bits (256 bytes) of data, and a 16-bit data CRC. The header field is permanently recorded and can not be written by the RX211.

### **OPERATION**

The RX211 controller has two registers: the Command and Status register and the Data Buffer register. The Data Buffer register is used to perform five different functions. When used to specify the diskette track, it is called the Track Address register. When used to specify the diskette sector, it is called the Sector Address register. When used to specify the number of data words to be transferred, i.e. the word count, it is called the Word Count register. When used to specify the starting memory address of the data to be transferred to or from memory, it is called the Bus Address register. When used to provide status information and specify errors, it is called the Error and Status register. When an error is detected, a READ ERROR CODE command will cause the controller to write four extended status words into memory. These extended status words contain detailed error and status information. (Refer to the register section at the back of this book for register and extended status word diagrams and bit definitions.)

To begin a READ operation, the processor loads the command and status register with a READ SECTOR command. The microprocessor controller responds with a request for the sector address by setting TRANSFER REQUEST <07> in the command and status register. The processor then loads the sector address into the data buffer register. The microprocessor controller next requests the track address by again setting TRANSFER REQUEST <07>, and the processor responds by loading the track address into the data buffer register. The READ operation has now been initiated.

The microprocessor controller positions the RX211 head to the track specified and reads each sector address from the sector header as it passes by on the rotating diskette until the specified sector is reached. The 2048 bits of data are then read and stored in the microprocessor's internal data buffer. When the data buffer is full, the microprocessor generates an interrupt to alert the processor that the data has been read off the diskette.

To transfer the data read off the diskette into memory, the processor loads the command and status register with an EMPTY BUFFER command. The microprocessor controller responds with a request for the number of data words to be transferred by setting TRANSFER REQUEST <07> in the command and status register. The processor then loads the word count into the data buffer register. The microprocessor next requests the starting memory address where the data read off the diskette is to be stored in memory by again setting TRANSFER REQUEST <07>, and the processor responds by loading the bus address into the data buffer register.

The microprocessor controller assembles the 2048 bits of data in its internal data buffer into 16-bit words and generates a parity bit for each word. Each 16-bit word plus parity is written into the memory location specified. This process continues until the proper word count is reached. Finally, the microprocessor generates an interrupt to alert the processor that the data read off the diskette has been stored in memory.

To begin a WRITE operation, the processor loads the command and status register with a FILL BUFFER command. The microprocessor controller responds with a request for the number of data words to be transferred by setting TRANSFER REQUEST <07>. The processor then loads the word count into the data buffer register. The microprocessor next requests the starting memory address of the data to be written onto the diskette by again setting TRANSFER REQUEST <07>, and the processor responds by loading the bus address into the data buffer register. The WRITE operation has now been initiated.

The microprocessor controller transfers the 16-bit words of data from memory, one by one, into its internal data buffer. This process continues until the proper word count is reached. The microprocessor generates an interrupt to alert the processor that the internal data buffer has been loaded.

To write the data onto the diskette, the processor loads a WRITE SECTOR command into the command and status register. The microprocessor controller responds with a request for the sector address by setting TRANSFER REQUEST <07>. The processor then loads the



sector address into the data buffer register. The microprocessor next requests the track address by again setting TRANSFER REQUEST <07>, and the processor responds by loading the track address into the data buffer register.

The microprocessor controller positions the RX211 head to the track specified and reads each sector address from the sector header as it passes by on the rotating diskette until the specified sector is reached. The microprocessor then serially writes the 2048 bits of data into the sector and generates an interrupt to alert the processor that the data has been written onto the diskette.

### **DATA INTEGRITY**

Several error checking and correction features of the RX211 ensure that the data is correct.

The RX211 locates the specified track and then reads the header information to verify that it is the specified track. The header CRC is used to ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the diskette. If there is a discrepancy between the two CRCs, the microprocessor controller alerts the processor via an error code in the extended status word 1.

The data CRC is used to ensure that the data field has been read correctly. The data bits are used to generate a second CRC, which is then compared to the CRC read from the end of the data field on the diskette. If there is a discrepancy between the two CRCs, the microprocessor controller alerts the processor by setting a bit in the error and status register.

### **INTERRUPTS**

The RX211 floppy disk subsystem microprocessor controller uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the command and status register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the ERROR or DONE bit in the command and status register is also set.

When the ERROR bit is set, it indicates that some error condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the DONE bit is set, the microprocessor controller has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the pro-

gram can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 264. Note that the priority level can be changed with a priority plug and the vector address can be changed by switches in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### RELIABILITY/MAINTAINABILITY

Reliability means long life expectancy and uninterrupted processing of the floppy disk subsystem. Special design features of the RX211 subsystems provide these qualities of high reliability as well as ease of maintenance.

- Modular construction of the RX211 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Long head and diskette life due to minimal contact since the head only touches the diskette during an operation.

### SPECIFICATIONS

#### MECHANICAL

Cabinet	Cabinet-mountable
Controller mounting code	One quad slot
Height	10.5 in (26.7 cm)
Width	19 in (48.3 cm)
Depth	17 in (43.2 cm)
Weight	60 lbs (27 kg)

#### PERFORMANCE

Drives per controller	2
Formatted capacity per diskette	0.5 MB
Peak transfer speed	61 KB/s
Average access time*	262 ms

\* Average access time is defined as the sum of the average seek time, the settling time, and the average latency (rotational) time.

## DISK DRIVES

Average seek time	154 ms
Average latency (rotational) time	83 ms
Settling time	25 ms
Track-to-track seek	6 ms
Rotational speed	360 rpm
Data surfaces per diskette	1
Tracks per diskette	77
Sectors per track	26
Bytes per sector	256 (8-bit format)
Tracks per inch	48
Bits per inch	3200

### **ELECTRICAL**

Operating current	4 A at 120 Vac 2 A at 240 Vac
Interface (controller) current	1.5 A at +5 Vdc
Power Consumption	500 Watts
Heat dissipation	1700 Btus/hr
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	60 Hz $\pm$ 0.5 Hz 50 Hz $\pm$ 0.5 Hz
Receptacles	NEMA #5-15R (120 Vac), NEMA #6-15R (240 Vac)
Line cord length	9 ft

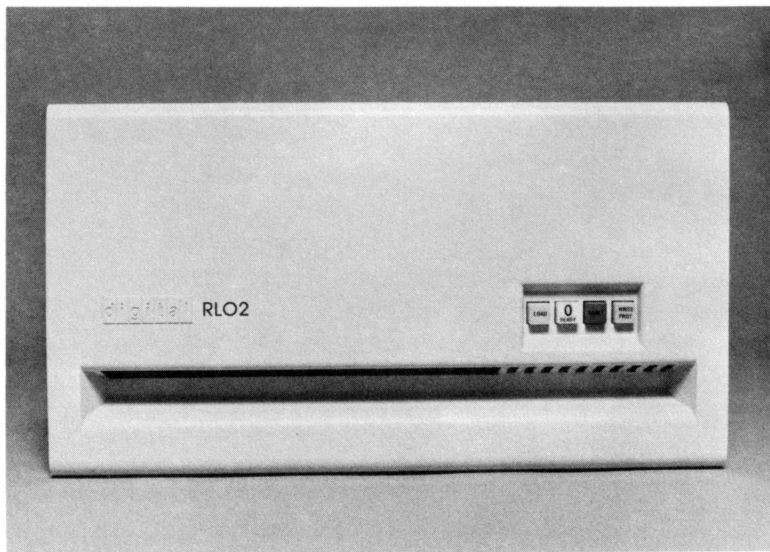
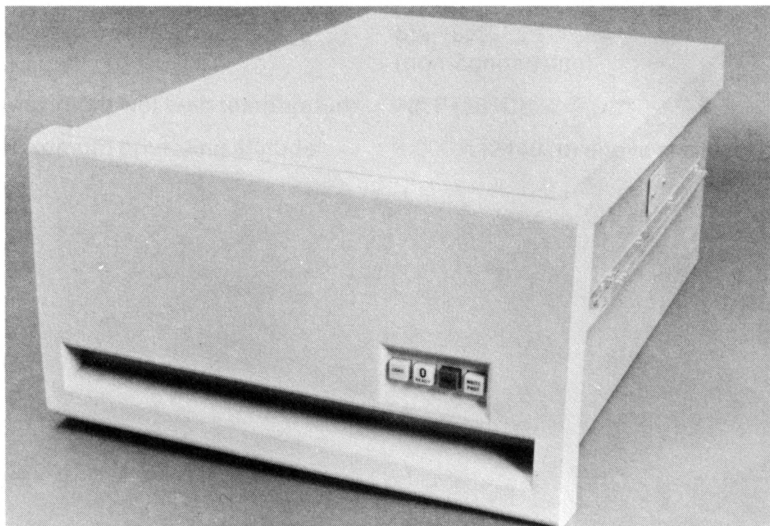
### **ENVIRONMENTAL**

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–151°F (-40°C–66°C)

*DISK DRIVES*

Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–98% (non-condensing)
Maximum wet bulb temperature	78°F (26°C)
Maximum operating altitude	8,000 ft (2440 m) above sea level





**RL01/02**

## **RL01/02**

The RL01/02 is a random-access, cartridge disk storage system which connects to the UNIBUS via the controller. The RL11-AK and RL211-AK subsystems are supported by UNIBUS PDP-11 systems. VAX-11/750 systems also support the RL211-AK subsystems, but only as a data file resident device for transport of data to and from other DIGITAL systems. The RL01/02 was designed to operate at medium speeds in moderate usage environments in a wide range of commercial, engineering, laboratory, educational, and even some industrial and military applications.

## **FEATURES**

- Formatted capacity of 10.4 MB (RL02) and 5.2 MB (RL01)
- Removable disk cartridge provides unlimited off-line storage
- Overlapped seeks optimize seek time and provide increased system throughput on multidrive systems
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 4 disk drives per subsystem

## **DESCRIPTION**

The RL11-AK subsystem consists of a toploading, RL01 cartridge disk drive, a controller, an I/O cable, and a disk cartridge. Up to three more add-on RL01-AK cartridge disk drives may be added to this subsystem. Each processor will support a maximum of two controllers. The RL211-AK subsystem consists of a toploading, RL02 cartridge disk drive, a controller, an I/O cable, and a disk cartridge. Up to three more add-on RL02-AK cartridge disk drives may be added to this subsystem. Each processor will support a maximum of two controllers.

## **RECORDING METHOD**

The RL01/02 utilizes Modified Frequency Modulation (MFM) to read and write data. Data is written on the disk by magnetizing small sections (bit cells) of the oxide on the disk in different directions, i.e. either positively or negatively. A change in the direction of magnetization (flux transition) in the clock area or the data area of a bit cell indicates whether the bit represented is a 1 or a 0.

## **DATA ORGANIZATION**

The RL01/02 disk cartridge consists of one disk platter, recorded on both sides, enclosed in a protective case. The RL01/02 has 2 heads which correspond to the 2 data surfaces. The RL02 disk cartridge is divided into 512 cylinders (256 for the RL01). Each cylinder is divided into 2 tracks, corresponding to the 2 data surfaces. Each track is divided into 40 sectors with a data storage capacity of 2048 bits (256

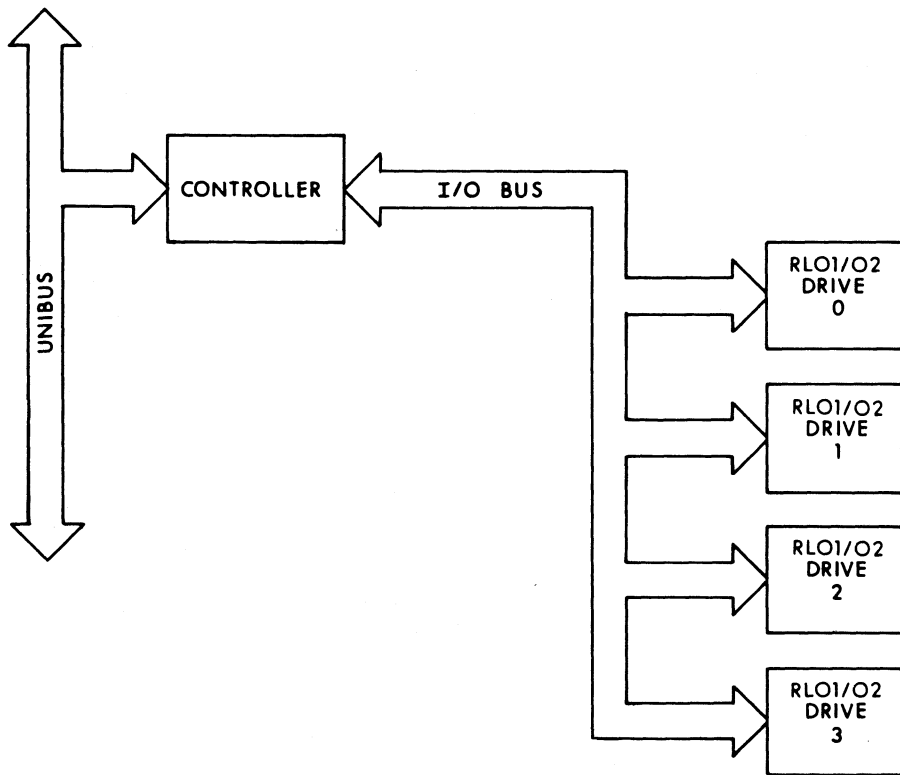


Figure 2-2 RL11/RL211 SYSTEM BLOCK DIAGRAM

DISK DRIVES



bytes). Each sector is divided into a servo field, a header field, and a data field. The header field consists of a 16-bit header that contains the cylinder, track, and sector addresses and a 16-bit header CRC (Cyclic Redundancy Check). The data field consists of 2048 bits (256 bytes) of data and a 16-bit data CRC. The sector field and the header field are permanently recorded and can not be rewritten by the disk drive.

## OPERATION

The RL11/RL211 subsystems have the following four registers: the Control and Status Register, the Bus Address Register, the Disk Address Register, and the Multipurpose Register. (Refer to the register section at the back of this book for register diagrams and bit definitions.)

Before a READ or a WRITE operation can begin, the processor must issue a SEEK command unless the heads are already positioned at the desired cylinder. To initiate a SEEK command, the processor loads the disk address register with the number of cylinders the heads are to be moved, the direction they are to be moved (toward or away from the spindle), and the head to be used (track 0 or 1). The control and status register is then loaded to select the drive number (0-3) and specify the SEEK command. The drive moves the heads the number of cylinders specified and generates an interrupt when the SEEK operation has been completed.

Once the heads are positioned at the desired cylinder, the processor loads the multipurpose, bus address, and disk address registers respectively. The multipurpose register specifies the number of words to be transferred between the disk and memory. The bus address register specifies the starting memory address of the location for the data to be read from or written onto the disk. The disk address register specifies the sector of the disk to be read or written.

After the multipurpose, bus address, and disk address registers have been loaded, the control and status register is loaded to specify the drive number (0-3) and whether this is to be a READ or WRITE operation. The READ or WRITE command is then executed. The specified head then reads the sector header fields to locate the specified sector on the rotating disk.

During a READ operation, data bits are read from the disk serially. The controller assembles the bits into 16-bit parallel words and generates a parity bit for each 16-bit word. The controller then transfers each 16-bit word plus parity to the specified memory location. This process continues until the specified number of words is reached or until the

end of the current track, whichever comes first. When the READ operation has been completed, an interrupt is generated to alert the processor that the data has been read off the disk and is stored in the specified memory location.

During a WRITE operation, the controller reads each 16-bit parallel word from the specified memory location and generates a parity bit for each 16-bit word. The controller then transfers each 16-bit word plus parity to the drive. The drive serially writes the bits onto the disk. This process continues until the specified number of words is reached or until the end of the current track, whichever comes first. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RL01/02 ensure that the data is correct.

During a data transfer operation, the RL01/02 reads the sector header field to verify that it has reached the specified cylinder, track, and sector. The header CRC is used to ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the disk. If there is a discrepancy between the two CRCs, the controller alerts the processor by setting a bit in the control and status register.

The data CRC is used to ensure that the data field has been read correctly. The data bits are used to generate a second CRC, which is then compared to the CRC read from the end of the data field on the disk. If there is a discrepancy between the two CRCs, the controller alerts the processor by setting a bit in the control and status register. If a sector contains an error, the processor issues a RETRY command.

To ensure that data is written correctly, a WRITE CHECK command may be issued by the software. This causes the RL01/02 to read the data just written and the RL01/02 controller to compare it to the data stored in memory.

### **INTERRUPTS**

The RL01/02 disk system controller uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the CONTROLLER READY or DRIVE READY bit in the control and status register is also set.

When the COMPOSITE ERROR bit is set in addition to the DRIVE READY bit, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the CONTROLLER READY bit is set, the controller has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 160. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### RELIABILITY/MAINTAINABILITY

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RL01/02 disk systems provide these qualities of high reliability as well as ease of maintenance.

- Modular construction of the RL01/02 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Easy access from the top of the drive to the subassemblies and heads.
- Track-following embedded servo system minimizes maintenance by eliminating drive head alignment.

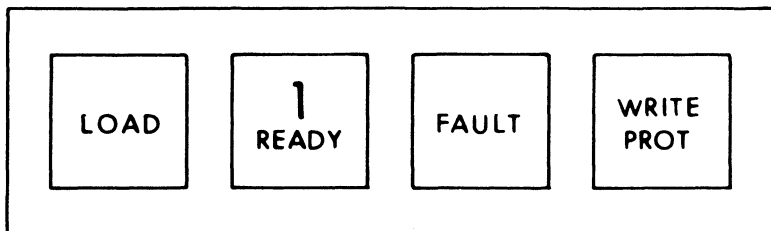


Figure 2-3 RL01/02 FRONT PANEL CONTROLS AND INDICATORS

**PANEL CONTROLS AND INDICATORS**

The front panel controls allow the operator to control the disk drive manually. The indicator lights provide drive status information.

- **LOAD switch** (alternate-action pushbutton/white light indicator on front panel)

Depressing this switch causes the indicator light to go out and the drive to accelerate the disk up to speed. Once the disk is up to speed, the **READY** indicator will light. Depressing the switch again causes the drive to stop the disk and the **LOAD** indicator to light.

- **DRIVE NUMBER receptacle/READY indicator** (unlabeled receptacle/white light indicator on front panel)

Each drive comes with four numbered (0-3) plugs. The drive number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, the drive cannot be selected by the processor. Note that drive number units cannot be duplicated.

When lit, the disk is up to speed and the drive is ready to execute a command.

- **FAULT indicator** (white light indicator on front panel)

When lit, the drive has detected a hardware fault such as write current failure or loss of system clock.

- **WRITE PROTECT switch** (alternate-action pushbutton/white light indicator on front panel)

Depressing this switch causes the indicator to light and prevents the processor from writing on the disk cartridge. Depressing this switch again causes the indicator light to go out and enables **WRITE** operations.

**SPECIFICATIONS****MECHANICAL**

Cabinet	Cabinet-mountable
Controller mounting code	One hex slot
Height	10.5 in (26.7 cm)
Width	19 in (48.3 cm)
Depth	25 in (63.5 cm)
Weight	75 lbs (33.8 kg)

**PERFORMANCE**

Drives per controller	4
Formatted capacity per disk cartridge	
RL01	5.2 MB
RL02	10.4 MB
Peak transfer speed	512 KB/s
Average access time*	67.5 ms
Average seek time	55 ms
Average latency (rotational) time	12.5 ms
Track-to-track seek	15 ms
Rotational Speed	2400 rpm
Surfaces per disk cartridge	2
Tracks per surface	
RL01	256
RL02	512
Sectors per track	40
Bytes per sector	256
Tracks per inch	250
Bits per inch	3725

**ELECTRICAL**

Starting (surge) current	5 A at 120 Vac 2.5 A at 240 Vac
Surge duration	10 s
Operating current	1.5 A at 120 Vac 0.8 A at 240 Vac

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

Controller (Interface) current	5 A at 5 Vdc, 0.5 A at +15 Vdc, 0.5 A at -15 Vdc
Power consumption	150 Watts
Heat dissipation	600 Btus/hr
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	60 Hz $\pm$ 3 Hz 50 Hz $\pm$ 2.5 Hz
Receptacles	NEMA #5-15R (120 Vac), NEMA #6-15R (240 Vac)
Line cord length	10 ft (3 m)

### **ENVIRONMENTAL**

Operating temperature	50°F–104°F (10°C–40°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Operating relative humidity	10%–90% (non-condensing)
Storage relative humidity	10%–95% (non-condensing)
Maximum wet bulb temperature	82°F (28°C)
Maximum operating altitude	8000 ft (2440 m) above sea level

## *DISK DRIVES*



**RK07**



## **RK07**

The RK07 is a freestanding, random-access, disk storage system which connects to the UNIBUS via the controller. The RK711 subsystems are supported by UNIBUS PDP-11 systems and VAX-11/780 systems. The RK07 was designed to operate at medium speeds in moderate usage environments in a variety of commercial and scientific applications.

## **FEATURES**

- Formatted capacity of 28 MB
- Removable disk cartridge provides unlimited off-line storage
- Overlapped seeks optimize seek time and provide increased system throughput on multidrive systems
- Static dual-access capability
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 8 disk drives per subsystem

## **DESCRIPTION**

The RK711-EA(ED) and RK711-PA(PD) disk storage subsystems consist of a single-access, freestanding RK07 disk drive, a controller, an I/O cable, and a disk cartridge. Up to seven more add-on RK07 drives (single- or dual-access) may be added to these subsystems. The RK711-EA(ED) subsystems and the RK07-EA(ED) add-on drives are compatible with UNIBUS PDP-11 and VAX-11/780 systems configured in H960 and H9600 series cabinets. The RK711-PA(PD) subsystems and the RK07-PA(PD) add-on drives are compatible with UNIBUS PDP-11 systems configured in H9640 series cabinets. The RK07-PA(PD) add-on drive may also be added to VAX-11/750 systems configured with an RK711 subsystem.

The RK711-FA(FD) disk storage subsystems consist of a dual-access, freestanding RK07 disk drive, two UNIBUS controllers, two I/O cables, and a disk cartridge. Up to seven more add-on RK07 disk drives (single- or dual-access) may be added to these subsystems. The RK711-FA(FD) subsystems and the RK07-FA(FD) add-on drives are compatible with UNIBUS PDP-11 and VAX-11/780 systems configured in H960 and H9600 series cabinets. Note that dynamic (simultaneous access) dual-port capability of disk subsystems is not supported by DIGITAL operating system software or diagnostics. However, the RK711-FA(FD) subsystems can be statically shared by two processors or connected to one processor through two UNIBUS controllers for maximum system availability.

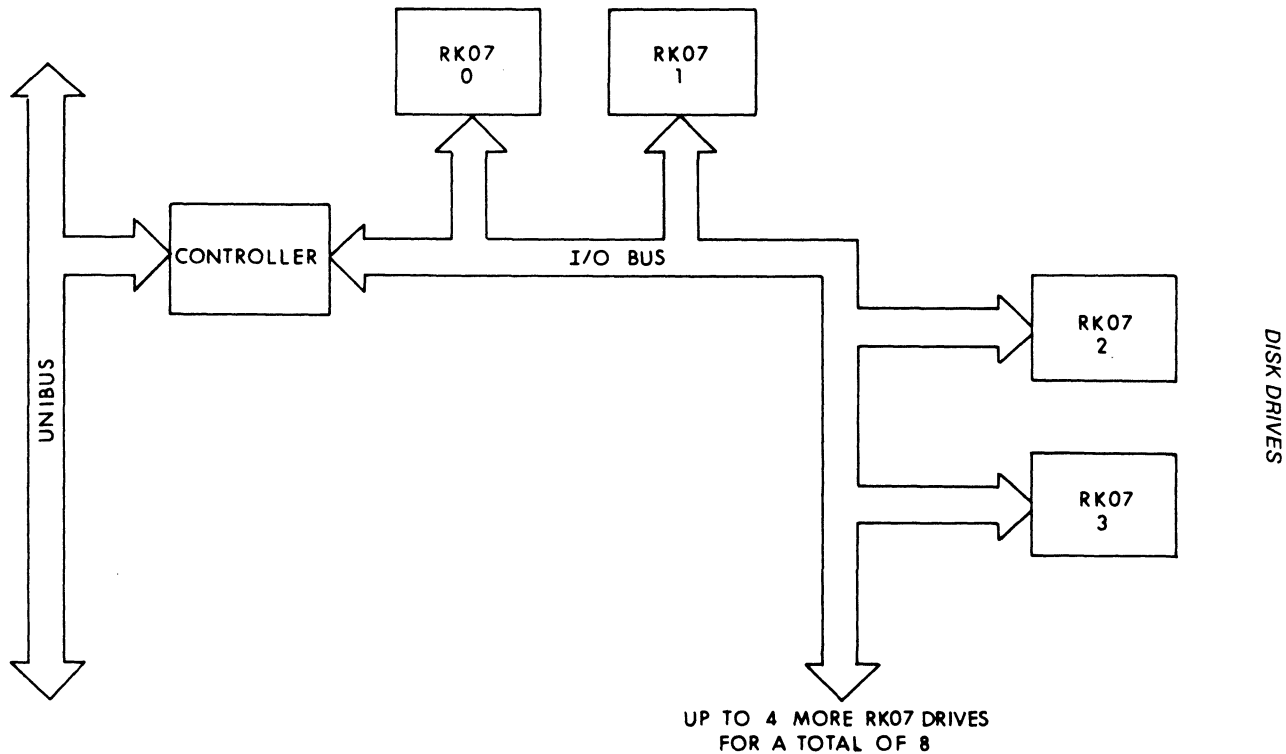


Figure 2-4 RK711 SYSTEM BLOCK DIAGRAM

**RECORDING METHOD**

The RK07 utilizes Modified Frequency Modulation (MFM) to read and write data. Data is written on the disk by magnetizing small sections (bit cells) of the oxide on the disk in different directions, i.e. either positively or negatively. A change in the direction of magnetization (flux transition) clock area or the data area of a bit cell indicates whether the bit represented is a 1 or a 0.

**DATA ORGANIZATION**

The RK07 disk cartridge consists of 2 disk platters, each recorded on both sides, enclosed in a protective cover. Each disk cartridge contains a total of 4 surfaces: 3 data surfaces for recording and 1 servo surface permanently recorded with information used to position the read/write heads at the specified cylinder. The RK07 has 4 heads—3 are read/write heads which correspond to the 3 data surfaces and the additional head is the servo read head, which corresponds to the servo surface. The disk cartridge is divided into 815 cylinders. Each cylinder is divided into 3 tracks, corresponding to the 3 data surfaces. Each track is divided into 22 sectors with a data storage capacity of 4096 bits (512 bytes). Each sector is divided into a preamble, a header field, and a data field. The header field consists of a 32-bit header that contains the cylinder, track, and sector addresses and a 16-bit header check word. The data field consists of 4096 bits (512 bytes) of data and a 32-bit data ECC (Error Correcting Code). The preamble and the header field can only be written by the utility program that formats these disk cartridges.

**OPERATION**

The RK711 subsystems have 15 registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ or a WRITE operation can begin, the processor loads the bus address, word count, control and status 2, desired cylinder, disk address, and control and status 1 registers respectively.

The bus address register specifies the starting memory address of the location for the data to be read from or written onto the disk. The word count register specifies the number of words to be transferred between the disk and memory. The control and status 2 register selects which of the disk drives (up to 8 per controller) is to perform the operation. The desired cylinder register and the disk address register specify the sector of the disk to be read or written.

After the bus address, word count, control and status 2, desired cylinder, and disk address registers have been loaded, the control and status 1 register is loaded with the READ or WRITE command from the

processor. The command is then executed. If the heads are not currently positioned at the specified cylinder, the drive will do an implied SEEK, which moves the heads to the correct cylinder. The read/write data heads then begin reading the headers on the specified track to locate the specified sector.

During a READ operation, data bits are read from the disk serially. The controller assembles the bits into 16-bit parallel words and generates a parity bit for each 16-bit word. The controller then transfers each 16-bit word plus parity to the specified memory location. This process continues until the proper word count is reached. When the READ operation has been completed, an interrupt is generated to alert the processor that the data has been read off the disk and is stored in the specified memory location.

During a WRITE operation, the controller reads each 16-bit parallel word from the specified memory location and generates a parity bit for each 16-bit word. The controller then transfers each 16-bit word plus parity to the drive. The drive serially writes the bits onto the disk. This process continues until the proper word count is reached. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RK07 ensure that the data is correct.

The RK07 uses the servo disk surface to position the read/write heads at the specified cylinder. The sector header field is read to verify that it is the specified cylinder, track, and sector. The header check word is used to ensure that the header field has been read correctly. The header bits are used to generate a second header check word, which is then compared to the word read from the end of the header field on the disk. If there is a discrepancy between the two header check words, the controller alerts the processor by setting a bit in the error register.

To ensure that data is written correctly, a WRITE CHECK command may be issued by the software. This causes the RK07 to read the data just written and the RK07 controller to compare it to the data stored in memory.

The ECC (Error Correction Code) logic is used to ensure that the data field has been read correctly. The data bits are used to generate a second ECC, which is then compared to the ECC read from the end of the data field on the disk. If there is a discrepancy between the two ECCs, the processor uses them to determine which bits are in error

and to reconstruct the correct data. One error of up to 11 incorrect bits in a row can be reconstructed in a sector. The controller reports the position of the error to the processor and sends the processor an error burst pattern and an error correction pattern to allow the software to correct the error in memory. If a sector containing more than one error is reported to the processor by the controller as an in-correctable error, the processor may invoke a suitable error recovery procedure consisting of OFFSET positioning, RECALIBRATION, and REREAD operations.

## **INTERRUPTS**

The RK07 disk system controller uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status 1 register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the COMBINED ERROR, DRIVE INTERRUPT, or CONTROLLER READY bit in the control and status 1 register is also set.

When the COMBINED ERROR or DRIVE INTERRUPT bits are set, they indicate that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the controller has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 210. Note that the priority level can be changed with a priority plug and the vector address can be changed by switches in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RK07 disk systems provide these qualities of high reliability as well as ease of maintenance.

- Modular construction and easy access to the subassemblies and heads of the RK07 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Off-line tester allows the RK07 to be serviced independent of the host processor.
- Light-emitting diodes on key status bits permit fast, easy error diagnosis and repair.

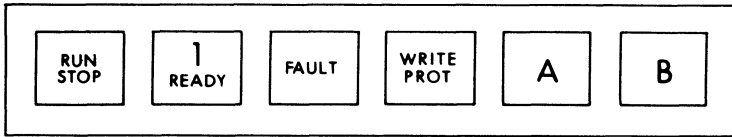


Figure 2-5 RK07 FRONT PANEL CONTROLS AND INDICATORS

### PANEL CONTROLS AND INDICATORS

The front panel controls allow the operator to control the disk drive manually. The indicator lights provide drive status information.

- RUN/STOP switch (alternate-action pushbutton/yellow light indicator on front panel)

Depressing this switch causes the indicator to light and the drive to accelerate the disk cartridge up to speed. Once the disk cartridge is up to speed, the READY indicator will light. Depressing the switch again causes the drive to stop the disk cartridge and the START indicator light to go out.

- DRIVE NUMBER receptacle/READY indicator (unlabeled receptacle/white light indicator on front panel)

Each drive comes with eight numbered (0-7) plugs. The drive number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, the drive cannot be selected by the processor. Note that drive number units cannot be duplicated.

When this READY indicator is lit, the disk cartridge is up to speed and the drive is ready to execute a command.

- FAULT indicator (red light indicator on front panel)

When lit, the drive has detected a hardware fault such as write current failure or a dc power supply failure.

- WRITE PROTECT switch (alternate-action pushbutton/yellow light indicator on front panel)

Depressing this switch causes the indicator to light and prevents the processor from writing on the disk cartridge. Depressing this switch again causes the indicator light to go out and enables WRITE operations.

- A and B switches (alternate-action pushbuttons/white light indicators on front panel)

Depressing switch A enables port A. Depressing switch B enables port B. When both switches are depressed both ports are enabled.

The A indicator lights when the drive is being accessed by port A and the B indicator lights when the drive is being accessed by port B.

**SPECIFICATIONS****MECHANICAL**

Cabinet	Freestanding
Controller mounting code	2 Sus
Height	
RK07-EA(ED), RK07-FA(FD)	39 in (99 cm)
RK07-PA(PD)	41.75 in (106 cm)
Width	
RK07-EA(ED), RK07-FA(FD)	21.7 in (55.2 cm)
RK07-PA(PD)	21.25 in (54.1 cm)
Depth	
RK07-EA(ED), RK07-FA(FD)	30 in (76.2 cm)
RK07-PA(PD)	30 in (76.2 cm)
Weight	
RK07-EA(ED), RK07-FA(FD)	326 lbs (148 kg)
RK07-PA(PD)	339 lbs (153.9 kg)

**PERFORMANCE**

Drives per controller	8
Formatted capacity per disk cartridge	28 MB
Peak transfer speed	538 KB/s
Average access time*	49 ms
Average seek time	36.5 ms
Average latency (rotational) time	12.5 ms
Track-to-track seek	6.5 ms
Rotational Speed	2400 rpm
Surfaces per disk cartridge	3 data, 1 servo
Tracks per surface	815

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

Sectors per track	22 (16-bit format)
Bytes per sector	512
Tracks per inch	384
Bits per inch	4040

### ELECTRICAL

Operating current	4 A at 120 Vac 2 A at 240 Vac
Controller (Interface) current	12 A at 5 Vdc, .18 A at +15 Vdc, .40 A at -15 Vdc
Power Consumption	500 Watts maximum (60 Hz) 550 Watts maximum (50 Hz)
Heat dissipation	1700 Btus/hr maximum (60 Hz) 1900 Btus/hr maximum (50 Hz)
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	60 Hz $\pm$ 3 Hz 50 Hz $\pm$ 3 Hz
Receptacles	NEMA #5-15R (120 Vac), NEMA #6-15R (240 Vac)
Line cord length	9 ft (2.7 m)

### ENVIRONMENTAL

Operating temperature	50°F–104°F (10°C–40°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Operating relative humidity	10%–90% (non-condensing)
Storage relative humidity	10%–95% (non-condensing)
Maximum wet bulb temperature	82°F (28°C)
Maximum operating altitude	8000 ft (2440 m) above sea level



*DISK DRIVES*



**RM02/03**

**RM02/03**

The RM02/03 is a freestanding, random-access, disk storage system which connects to the processor via the MASSBUS controller/adapter. The RJM02 subsystems are supported by UNIBUS PDP-11 systems except the PDP-11/70, the RWM03 subsystems are supported by PDP-11/70 systems, the REM03 subsystems are supported by VAX-11/780 systems, and the RGM03 subsystems are supported by VAX-11/750 systems. The RM02/03 was designed to operate at high speeds in high usage environments in a variety of applications.

**FEATURES**

- Formatted capacity of 67 MB
- Removable disk pack provides unlimited off-line storage
- Overlapped seeks optimize seek time and provide increased system throughput on multidrive systems
- Static dual-access capability
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 8 disk drives per subsystem

**DESCRIPTION**

The RJM02-AA(AD) disk storage subsystems consist of a single-access, freestanding RM02 disk drive, a MASSBUS controller, a MASSBUS cable, and a disk pack. Up to seven more add-on RM02 disk drives (single- or dual-access) may be added to these subsystems. The RWM03-AA(AD), REM03-AA(AD), and RGM03-AA(AD) disk storage subsystems consist of a single-access, freestanding RM03 disk drive, a MASSBUS controller/adapter, a MASSBUS cable, and a disk pack. Up to seven more add-on RM03 disk drives (single- or dual-access) may be added to these subsystems.

The RJM02-BA(BD) disk storage subsystems consist of a dual-access, freestanding RM02 disk drive, two MASSBUS controllers, two MASSBUS cables, and a disk pack. Up to seven more add-on RM02 disk drives (single- or dual-access) may be added to these subsystems. The RWM03-BA(BD), REM03-BA(BD), and RGM03-BA(BD) disk storage subsystems consist of a dual-access, freestanding RM03 disk drive, two MASSBUS controllers/adapters, two MASSBUS cables, and a disk pack. Up to seven more add-on RM03 disk drives (single- or dual-access) may be added to these subsystems. Note that dynamic (simultaneous access) dual-port capability of disk subsystems is not supported by DIGITAL operating system software or diagnostics. However, the RJM02-BA(BD), RWM03-BA(BD), REM03-BA(BD), and the RGM03-BA(BD) subsystems can be statically shared by two processors or connected to one processor through two MASSBUS controllers/adapters for maximum system availability.

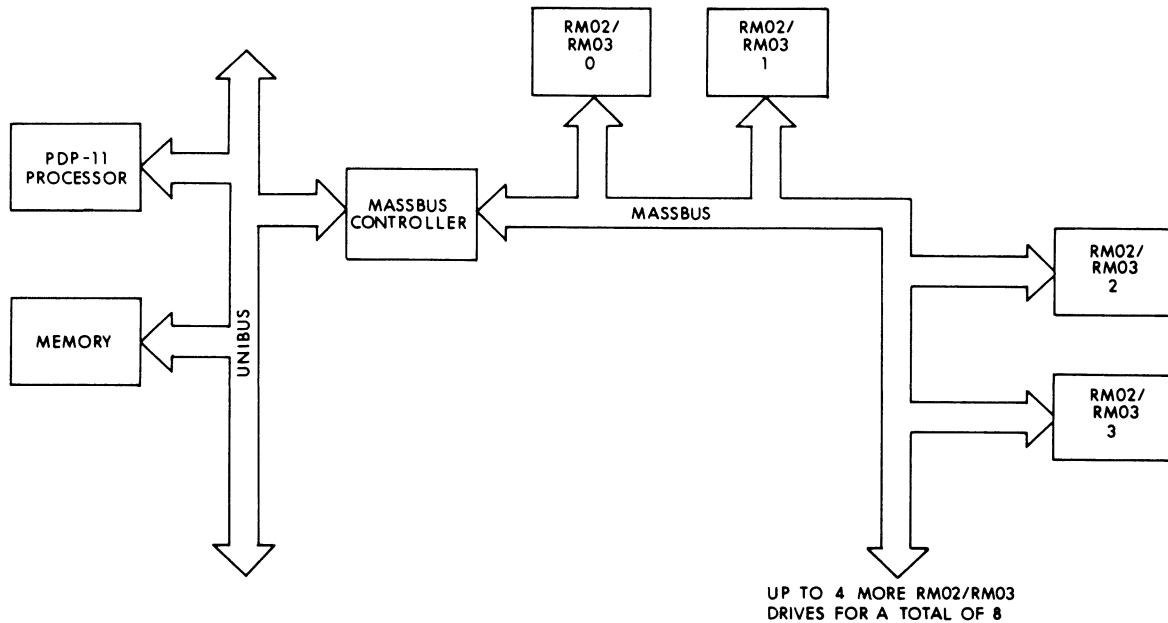


Figure 2-6 RJM02 SYSTEM BLOCK DIAGRAM

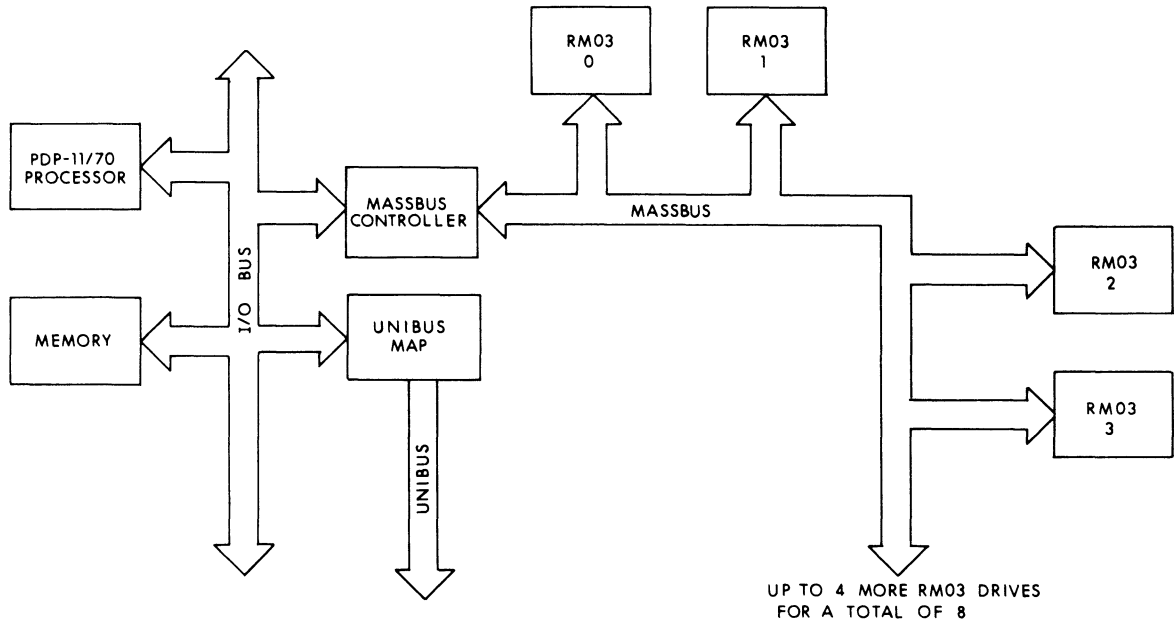
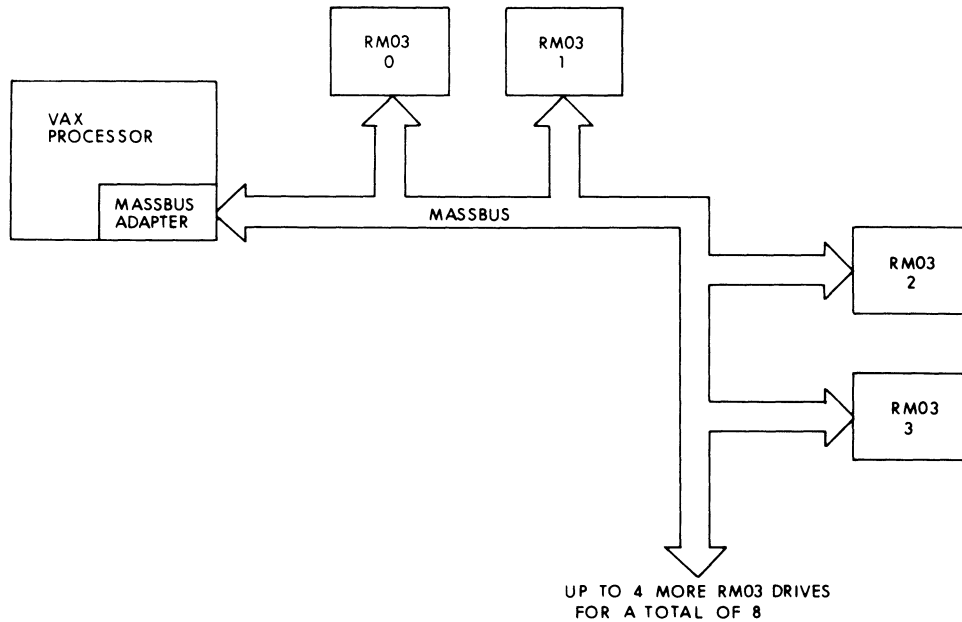


Figure 2-7 RWM03 SYSTEM BLOCK DIAGRAM



DISK DRIVES

Figure 2-8 REM03/RGM03 SYSTEM BLOCK DIAGRAM

## **RECORDING METHOD**

The RM02/03 utilizes Modified Frequency Modulation (MFM) to read and write data. Data is written on the disk by magnetizing small sections (bit cells) of the oxide on the disk in different directions, i.e. either positively or negatively. A change in the direction of magnetization (flux transition) in the clock area of a bit cell indicates whether the bit represented is a 1 or a 0.

## **DATA ORGANIZATION**

The RM02/03 disk pack consists of 3 disk platters, each recorded on both sides, enclosed between two outside platters for protection of the pack. Each disk pack contains a total of 6 surfaces: 5 data surfaces for recording and 1 servo surface permanently recorded with information used to position the read/write heads at the specified cylinder. The RM02/03 has 6 heads—5 are read/write heads which correspond to the 5 data surfaces and the additional head is the servo read head, which corresponds to the servo surface. The disk pack is divided into 823 cylinders. Each cylinder is divided into 5 tracks, corresponding to the 5 data surfaces. Each track is divided into 32 sectors with a data storage capacity of 4096 bits (512 bytes). Each sector is divided into a header field and a data field. The header field consists of an 48-bit header that contains the cylinder, track, and sector addresses and a 16-bit header CRC (Cyclic Redundancy Check). The data field consists of 4096 bits (512 bytes) of data and a 32-bit data ECC (Error Correction Code). The preamble and the header field can only be written by the utility program that formats these disk packs.

## **OPERATION**

The RJM02 subsystems have 20 registers, the RWM03 subsystems have 22 registers, and the REM03 and RGM03 subsystems have 16 registers plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ or a WRITE operation can begin, the processor loads the bus address, word count, control and status 2, desired cylinder, desired sector/track address, and control and status 1 registers respectively.

The bus address register specifies the starting memory address of the location for the data to be read from or written onto the disk. The word count register specifies the number of words to be transferred between the disk and memory. The control and status 2 register selects which of the disk drives (up to 8 per controller) is to perform the operation. The desired cylinder register and the desired sector/track address register specify the sector of the disk to be read or written.

After the bus address, word count, control and status 2, desired cylinder, and desired sector/track address registers have been loaded, the control and status 1 register is loaded with the READ or WRITE command from the processor. The command is then executed. If the heads are not currently positioned at the specified cylinder, the drive will do an implied SEEK, which moves the heads to the correct cylinder. The read/write heads then read the headers on the specified track to locate the specified sector.

During a READ operation, data bits are read from the disk serially. The controller/adaptor assembles the bits into 16-bit parallel words and generates a parity bit for each 16-bit word. The controller/adaptor then transfers each 16-bit word plus parity to the specified memory location. This process continues until the proper word count is reached. When the READ operation has been completed, an interrupt is generated to alert the processor that the data has been read off the disk and is stored in the specified memory location.

During a WRITE operation, the controller/adaptor reads each 16-bit parallel word from the specified memory location and generates a parity bit for each. The controller/adaptor transfers each 16-bit word plus parity to the drive. The drive then serially writes the bits onto the disk. This process continues until the proper word count is reached. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RM02/03 ensure that the data is correct.

The RM02/03 uses the servo disk surface to position the read/write heads at the specified cylinder. The sector header field is read to verify that it is the specified cylinder, track, and sector. The header CRC is used to ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the disk. If there is a discrepancy between the two CRCs, the controller/adaptor alerts the processor by setting a bit in the error 1 register.

To ensure that data is written correctly, a WRITE CHECK command may be issued by the software. This causes the RM02/03 to read the data just written and the controller/adaptor to compare it to the data stored in memory.

The ECC (Error Correction Code) logic is used to ensure that the data field has been read correctly. The data bits are used to generate a second ECC, which is then compared to the ECC read from the end of



the data field on the disk. If there is a discrepancy between the two ECCs, the processor uses them to determine which bits are in error and to reconstruct the correct data. One error of up to 11 incorrect bits in a row can be reconstructed in a sector. The controller/adaptor reports the position of the error to the processor and sends the processor an error burst pattern and an error correction pattern to allow the software to correct the error in memory. If a sector containing more than one error is reported to the processor by the controller/adaptor as an inconvertible error, the processor may invoke a suitable error recovery procedure consisting of OFFSET positioning, RECALIBRATION, and REREAD operations.

### **INTERRUPTS**

The RM02/03 disk system controller/adaptor uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status 1 register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the SPECIAL CONDITION or READY bit in the control and status 1 register is also set.

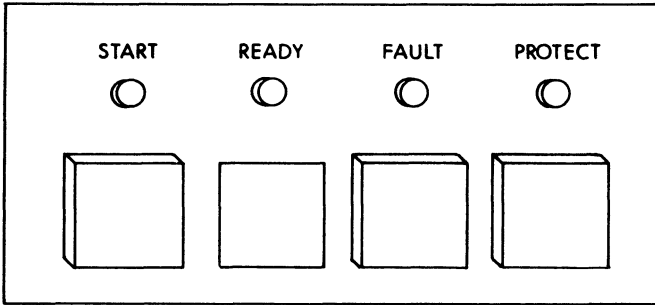
When the SPECIAL CONDITION bit is set, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the controller/adaptor has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 254. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

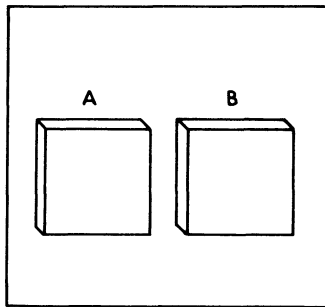
### **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RM02/03 disk systems provide these qualities of high reliability as well as ease of maintenance.

- Modular construction of the RM02/03 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Off-line tester allows the RM02/03 to be serviced independent of the host processor.
- Fault-isolation diagnostics simplify troubleshooting and provide extended maintenance and serviceability.



**FRONT PANEL CONTROLS AND INDICATORS**



**DRIVE CABINET SWITCHES**

Figure 2-9 RM02/03 CONTROLS AND INDICATORS

**CONTROLS AND INDICATORS**

The front panel controls allow the operator to control the disk drive manually and the indicator lights provide drive status information. The A and B switches located on the drive cabinet door allow the operator to enable different MASSBUS ports.

- **START switch and associated lamp (alternate-action pushbutton and associated red light indicator on front panel)**

Depressing this switch causes the START indicator light to come on and the drive to accelerate the disk pack up to speed. Once the disk pack is up to speed, the READY indicator will light. Depressing the switch again causes the drive to stop the disk pack and the START indicator light to go out.

- **READY lamp (red light indicator on front panel)**

When lit, indicates that the disk pack is up to speed and the drive is ready to execute a command. This lamp will blink during start/stop sequences.

- **DRIVE NUMBER receptacle (unlabeled receptacle on front panel)**

Each drive comes with eight numbered (0-7) plugs. The drive number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, the drive cannot be selected by the processor. Note that drive number units cannot be duplicated.

- **FAULT CLEAR switch and associated lamp (momentary pushbutton and associated red light indicator on front panel)**

Depressing this switch causes the indicator light to go out if the fault condition has been corrected.

When lit, the drive has detected a hardware fault such as write current failure or a dc power supply failure.

- **WRITE PROTECT switch and associated lamp (alternate-action pushbutton and associated red light indicator on front panel)**

Depressing this switch causes the associated indicator to light and prevents the processor from writing on the disk pack. Depressing this switch again causes the indicator light to go out and enables WRITE operations.

- **A and B switches/lamps (alternate-action pushbuttons/red light indicators on drive cabinet door)**

Depressing the A switch enables MASSBUS port A. Depressing the B switch enables MASSBUS port B. When both switches are depressed or when neither switch is depressed, both MASSBUS ports are enabled.

The A indicator lights when the drive is being accessed by MASSBUS port A and the B indicator lights when the drive is being accessed by MASSBUS port B.

**SPECIFICATIONS****MECHANICAL**

Cabinet	Freestanding
Controller/adaptor mounting code	
RJM02	2 SUs
RWM03	MASSBUS port
REM03	Option panel space
RGM03	MBA slot
Height	39 in (99 cm)
Width	21.7 in (55.1 cm)
Depth	31 in (79 cm)
Weight	430 lbs (195 kg)

**PERFORMANCE**

Drives per controller/adaptor	8
Formatted capacity per disk pack	67 MB
Peak transfer speed	
RM02	806 KB/s
RM03	1200 KB/s
Average access time*	
RM02	42.5 ms
RM03	38.3 ms
Average seek time	30 ms
Average latency (rotational) time	
RM02	12.5 ms

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

RM03	8.3 ms
Track-to-track seek	6 ms
Rotational speed	
RM02	2400 rpm
RM03	3600 rpm
Surfaces per disk pack	5 data, 1 servo
Tracks per surface	823
Sectors per track	32 (16-bit format)
Bytes per sector	512
Tracks per inch	384
Bits per inch	6038

### **ELECTRICAL**

Starting (surge) current	30 A at 120 Vac 22 A at 240 Vac
Surge duration	10-12 s
Drive operating current	11 A at 120 Vac 5.3 A at 240 Vac
Power consumption	1050 Watts maximum
Heat dissipation	4128 Btus/hr maximum
Drive operating voltage	120 Vac +8, -18 240 Vac +17, -27
Phase	1-phase
Line frequency	60 Hz +0.6, -1 50 Hz +0.5, -1
Drive receptacles	NEMA #5-15R (120 Vac), NEMA #6-15R (240 Vac)
Line cord length	6 ft

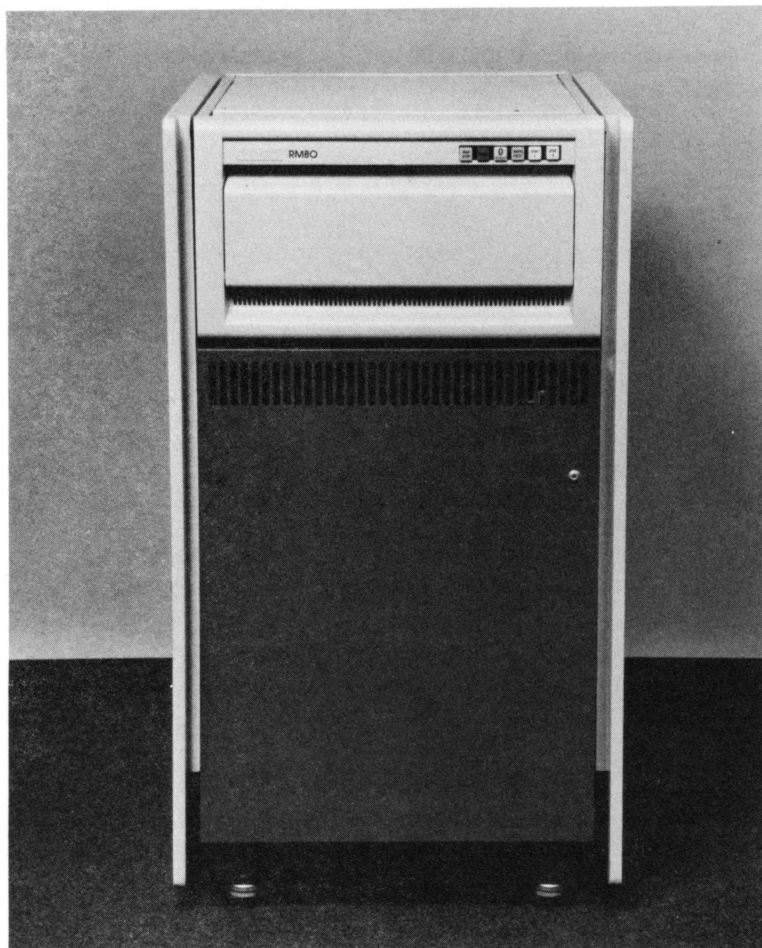
### **ENVIRONMENTAL**

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–158°F (-40°C–70°C)

## *DISK DRIVES*

<b>Operating relative humidity</b>	<b>20%–80%</b> <b>(non-condensing)</b>
<b>Storage relative humidity</b>	<b>5%–95%</b> <b>(non-condensing)</b>
<b>Maximum wet bulb temperature</b>	<b>78°F (26°C)</b>
<b>Maximum operating altitude</b>	<b>6500 ft (2000 m) above sea level</b>

## *DISK DRIVES*



**RM80**



## **RM80**

The RM80 is a freestanding, random-access, disk storage system which connects to the processor via the MASSBUS adapter (MBA). The REM80 subsystems are supported by VAX-11/780 systems and the RGM80 subsystems are supported by VAX-11/750 systems. The RM80 was designed to operate at very high speeds in high usage environments in a wide range of applications.

## **FEATURES**

- Formatted capacity of 124 MB
- Winchester fixed-media technology
- Sealed Head Disk Assembly (HDA)
- Internal microprocessor-controlled diagnostics
- Overlapped seeks optimize seek time and provide increased system throughput on multdrive systems
- Static dual-access capability
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 8 disk drives per subsystem

## **DESCRIPTION**

The REM80-AA(AD) and RGM80-AA(AD) disk storage subsystems consist of a single-access, freestanding RM80 disk drive with non-removable head disk assembly, a MASSBUS adapter (MBA), and a MASSBUS cable. Up to seven more add-on RM80 disk drives (single- or dual-access) may be added to these subsystems.

The REM80-BA(BD) and RGM80-BA(BD) disk storage subsystems consist of a dual-access, freestanding RM80 disk drive with non-removable head disk assembly, two MASSBUS adapters (MBAs), and two MASSBUS cables. Up to seven more add-on RM80 disk drives (single- or dual-access) may be added to these subsystems. Note that dynamic (simultaneous access) dual-port capability of disk subsystems is not supported by DIGITAL operating system software or diagnostics. However, the REM80-BA(BD) and RGM80-BA(BD) subsystems can be statically shared by two processors or connected to one processor through two MBAs for maximum system availability.

## **RECORDING METHOD**

The RM80 utilizes Modified Frequency Modulation (MFM) to read and write data. Data is written on the disk by magnetizing small sections (bit cells) of the oxide on the disk in different directions, i.e. either positively or negatively. A change in the direction of magnetization (flux transition) in the clock area of a bit cell indicates whether the bit represented is a 1 or a 0.

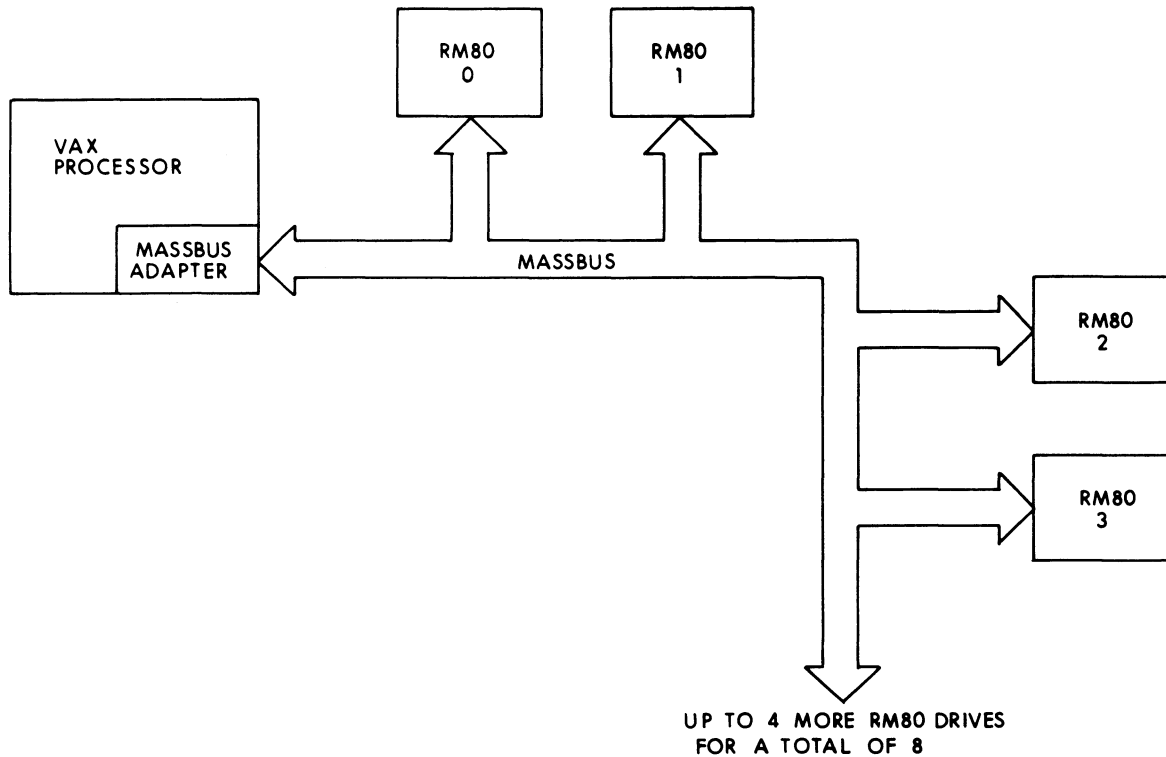


Figure 2-10 REM80/RGM80 SYSTEM BLOCK DIAGRAM

## DATA ORGANIZATION

The RM80 head disk assembly consists of 4 disk platters, each recorded on both sides. Each head disk assembly contains a total of 8 surfaces: 7 data surfaces for recording and 1 servo surface permanently recorded with information used to position the read/write heads at the specified cylinder. The RM80 has 15 heads—14 are read/write heads (two per data surface) and the additional head is the servo read head, which corresponds to the servo surface. The head disk assembly is divided into 561 cylinders: 559 are used for data and 2 are used for diagnostics. Each cylinder is divided into 14 tracks (two per data surface). Each track is divided into 32 sectors: 31 data sectors and one additional sector used when one of the sectors on that track is bad. Each sector has a data storage capacity of 4096 bits (512 bytes). Each sector is divided into a header field and a data field. The header field consists of a 48-bit header that contains the cylinder, track, and sector addresses and a 16-bit header CRC (Cyclic Redundancy Check). The data field consists of 4096 bits (512 bytes) of data and a 32-bit data ECC (Error Correction Code). The header field can only be written by the utility program that formats these head disk assemblies.

## OPERATION

The REM80 and the RGM80 subsystems have sixteen registers plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ or WRITE operation can begin, the processor loads the MBA virtual address, MBA byte counter, desired cylinder, desired sector/track address, and control and status 1 registers respectively.

The MBA virtual address register specifies the starting memory address of the storage location for the data to be read from or written onto the disk. The MBA byte counter register specifies the total number of bytes to be transferred between the disk and memory. The desired cylinder register and the desired sector/track address register specify the sector of the disk to be read or written.

After the MBA virtual address, MBA byte counter, desired cylinder, and desired sector/track address registers have been loaded, the control and status 1 register is loaded with the READ or WRITE command from the processor. The command is then executed. If the heads are not currently positioned at the specified cylinder, the drive will do an implied SEEK, which moves the heads to the correct cylinder. The read/write data heads then read the headers on the specified track to locate the specified sector.

During a READ operation, data bits serially read from the disk are assembled into 16-bit parallel words and a parity bit is generated for each 16-bit word. Every 16-bit word plus parity is then transferred to the MBA. The MBA combines two 16-bit words into a 32-bit memory word and generates a parity bit for each 32-bit word. Every 32-bit word plus parity is then transferred into the memory location specified. This process continues until the byte count in the MBA virtual address register is reached. When the READ operation is completed, an interrupt is set to alert the processor that the data has been read off the disk and stored in the specified memory location.

During a WRITE operation, each 32-bit word of data is read from memory and transferred to the MBA, which divides the 32-bit word into two 16-bit parallel words and generates a parity bit for each 16-bit word. The MBA then transfers the two 16-bit words plus parity to the drive. The drive checks the parity and then serially writes the bits onto the disk one by one. This process continues until the proper word count is reached. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RM80 ensure that the data is correct.

The RM80 uses the servo disk surface to position the read/write heads at the specified cylinder. The sector header field is read to verify that it is the specified cylinder, track, and sector. The header CRC is used to ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the disk. If there is a discrepancy between the two CRCs, the MBA alerts the processor by setting a bit in the error 1 register.

To ensure that data is written correctly, a WRITE CHECK command may be issued by the software. This causes the RM80 to read the data just written and the MBA to compare it to the data stored in memory.

The ECC (Error Correction Code) logic is used to ensure that the data field has been read correctly. The data bits are used to generate a second ECC, which is then compared to the ECC read from the end of the data field on the disk. If there is a discrepancy between the two ECCs, the processor uses them to determine which bits are in error and to reconstruct the correct data. One error of up to 11 incorrect bits in a row can be reconstructed in a sector. The MBA reports the position of the error to the processor and sends the processor an error

burst pattern and an error correction pattern to allow the software to correct the error. If a sector contains more than one error, the MBA alerts the processor by setting a bit in the error 1 register.

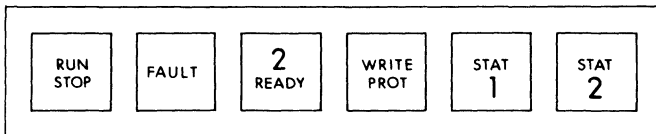
### INTERRUPTS

The RM80 disk system MBA uses a vectored interrupt to cause the program to branch to an interrupt service routine. The RM80 generates an interrupt at the completion of an operation, when an error has been detected, or when a drive comes on-line.

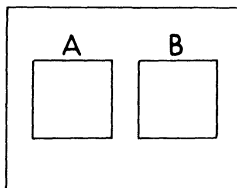
### RELIABILITY/MAINTAINABILITY

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RM80 disk systems provide these qualities of high reliability as well as ease of maintenance.

- Hinge-mounted modules for easy access.
- Winchester technology (Sealed Head Disk Assembly) requires no alignment of the heads.
- Modular construction of the RM80 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- On-line microprocessor-controlled diagnostic capability allows faults to be quickly isolated and corrected.



**FRONT PANEL CONTROLS AND INDICATORS**



**DRIVE CABINET SWITCHES**

Figure 2-11 RM80 CONTROLS AND INDICATORS

## CONTROLS AND INDICATORS

The front panel controls allow the operator to control the disk drive manually and the indicator lights provide drive status information. The A and B switches located on the drive cabinet door allow the operator to enable different MASSBUS ports.

- **RUN/STOP switch** (alternate-action pushbutton/yellow light indicator on front panel)

Depressing this switch causes the indicator to light and the drive to accelerate the head disk assembly up to speed. Once the head disk assembly is up to speed, the READY indicator will light. Depressing the switch again causes the drive to stop the head disk assembly and the START indicator light to go out.

- **FAULT switch** (momentary pushbutton/red light indicator on front panel)

When lit, the drive has detected a hardware fault such as write current failure or a dc power supply failure.

Depressing this switch causes the indicator light to go out if the fault condition has been corrected.

- **DRIVE NUMBER receptacle/READY indicator** (unlabeled receptacle/white light indicator on front panel)

Each drive comes with eight numbered (0-7) plugs. The drive number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, the drive cannot be selected by the processor. Note that drive number units cannot be duplicated.

When this READY indicator is lit, the head disk assembly is up to speed and the drive is ready to execute a command.

- **WRITE PROTECT switch** (alternate-action pushbutton/yellow light indicator on front panel)

Depressing this switch causes the indicator to light and prevents the processor from writing on the head disk assembly. Depressing this switch again causes the indicator light to go out and enables WRITE operations.

- **STAT 1 and STAT 2 lamps** (white light indicators on front panel)

These two indicators, in conjunction with the FAULT, READY, and WRITE PROTECT indicators, allow the drive to display 5-bit binary error code messages.

- **A and B switches** (alternate-action pushbuttons/white light indicators on drive cabinet door)

Depressing switch A enables MASSBUS port A. Depressing switch B enables MASSBUS port B. When both switches are depressed or

when neither switch is depressed, both MASSBUS ports are enabled.

The A indicator lights when the drive is being accessed by MASSBUS port A and the B indicator lights when the drive is being accessed by MASSBUS port B.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Freestanding
Controller mounting code	
REM80	Option panel space
RGM80	MBA slot
Height	39 in (99 cm)
Width	21.5 in (54.6 cm)
Depth	33 in (83.8 cm)
Weight	370 lbs (167 kg)

### PERFORMANCE

Drives per controller	8
Formatted capacity per head disk assembly	124 MB
Peak transfer speed	1200 KB/s
Average access time*	33.3 ms
Average seek time	25 ms
Average latency (rotational) time	8.3 ms
Track-to-track seek	6 ms
Rotational speed	3600 rpm
Surfaces per head disk assembly	7 data, 1 servo
Tracks per surface	1118 data and +4 for diagnostic testing

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

Sectors per track	31 data and +1 additional sector to replace a bad sector (16-bit format)
Bytes per sector	512
Tracks per inch	480
Bits per inch	6339

### **ELECTRICAL**

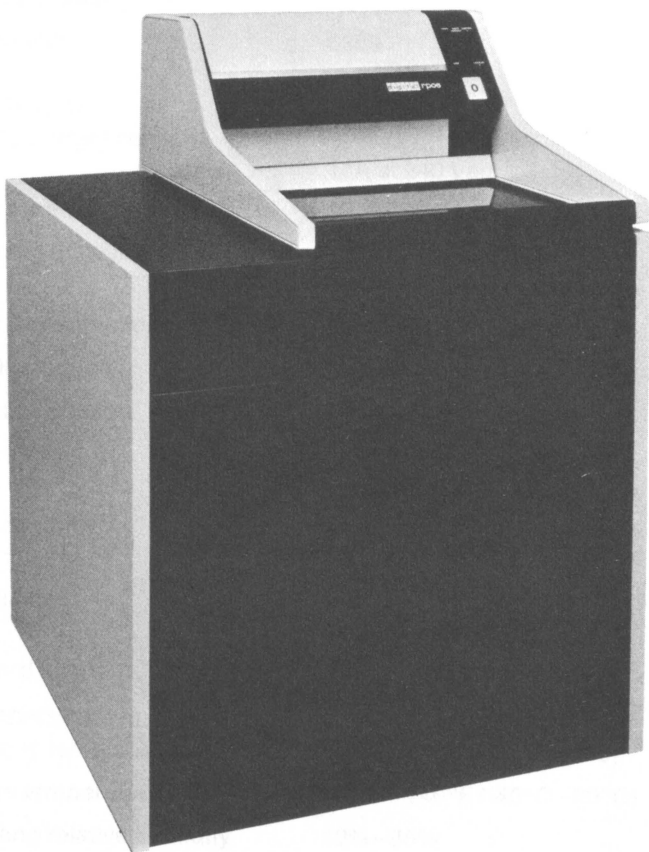
Starting (surge) current	35 A at 120 Vac 17A at 240 Vac
Surge duration	5 s
Operating current	7.5 A at 120 Vac 5 A at 240 Vac
Power Consumption	640 Watts
Heat dissipation	2185 Btus/hr
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	60 Hz $\pm$ 1 Hz 50 Hz $\pm$ 1 Hz
Receptacles	NEMA #5-15R (120 Vac), NEMA #6-15R (240 Vac)
Line cord length	7 ft

### **ENVIRONMENTAL**

Operating temperature	50°F–104°F (10°C–40°C)
Storage temperature	-40°F–140°F (-40°C–60°C)
Operating relative humidity	10%–85% (non-condensing)
Storage relative humidity	10%–85% (non-condensing)
Maximum wet bulb temperature	82°F (28°C)
Maximum operating altitude	8000 ft (2400 m) above sea level







**RP06**

## **RP06**

The RP06 is a freestanding, random-access, disk storage system which connects to the processor via the MASSBUS controller/adaptor. The RJP06 subsystems are supported by UNIBUS PDP-11 systems except the PDP-11/70, the RWP06 subsystems are supported by PDP-11/70 systems only, the REP06 subsystems are supported by VAX-11/780 systems, and the RGP06 subsystems are supported by VAX-11/750 systems. The RP06 was designed to operate at high speeds in high usage environments in a variety of applications requiring data security, system interchange, and personal databases.

## **FEATURES**

- Formatted capacity of 176 MB
- Removable disk pack provides unlimited off-line storage
- Overlapped seeks optimize seek time and provide increased system throughput on multidrive systems
- Static dual-access capability
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 8 disk drives per subsystem

## **DESCRIPTION**

The RJP06-AA(AB), RWP06-AA(AB), REP06-AA(AB), and RGP06-AA(AB) disk storage subsystems consist of a single-access, freestanding RP06 disk drive, a MASSBUS controller/adaptor, a MASSBUS cable, and a disk pack. Up to seven more add-on RP06 drives (single- or dual-access) may be added to any of these subsystems.

The RJP06-BA(BB), RWP06-BA(BB), REP06-BA(BB), and RGP06-BA(BB) disk storage subsystems consist of a dual-access, freestanding RP06 disk drive, two MASSBUS controllers/adaptors, and two MASSBUS cables. Up to seven more add-on RP06 disk drives (single- or dual-access) may be added to these subsystems. Note that dynamic (simultaneous access) dual-port capability of disk subsystems is not supported by DIGITAL operating system software or diagnostics. However, the RJP06-BA(BB), RWP06-BA(BB), REP06-BA(BB), and the RGP06-BA(BB) subsystems can be statically shared by two processors or connected to one processor through two MASSBUS controllers/adaptors for maximum system availability.

## **RECORDING METHOD**

The RP06 utilizes Modified Frequency Modulation (MFM) to read and write data. Data is written on the disk by magnetizing small sections (bit cells) of the oxide on the disk in different directions, i.e. either positively or negatively. A change in the direction of magnetization

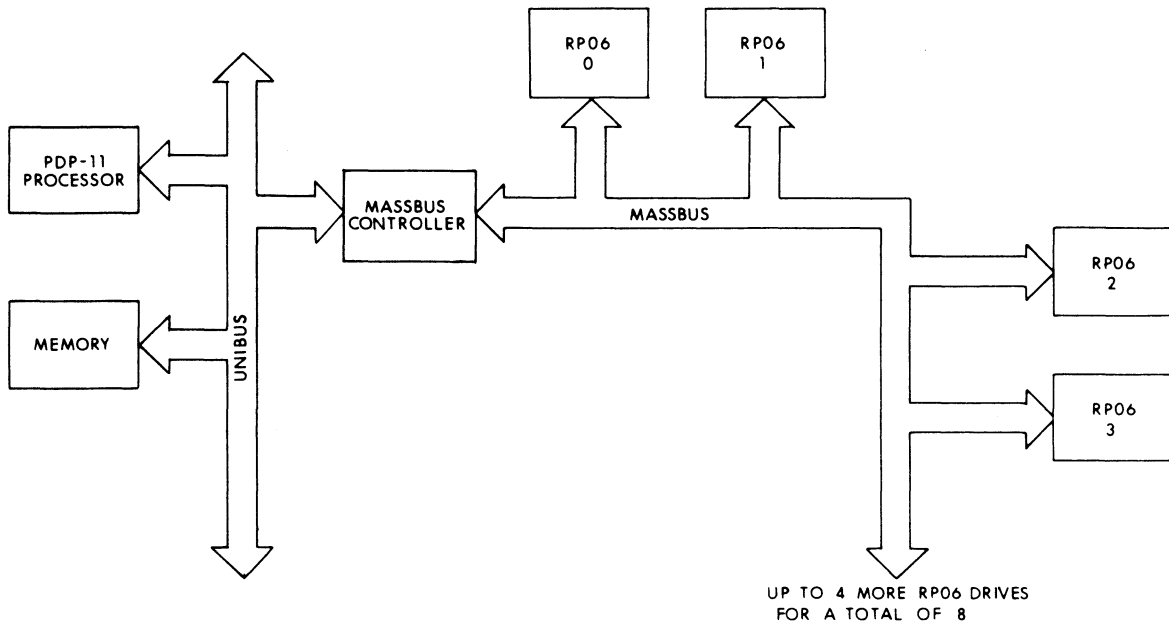


Figure 2-12 RJP06 SYSTEM BLOCK DIAGRAM

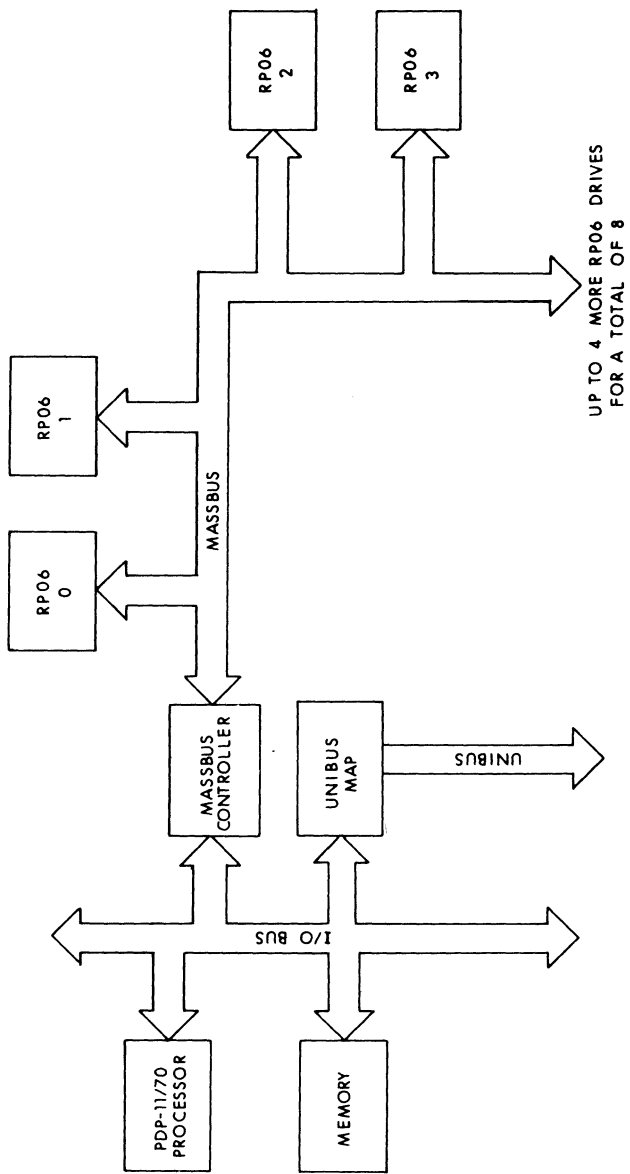
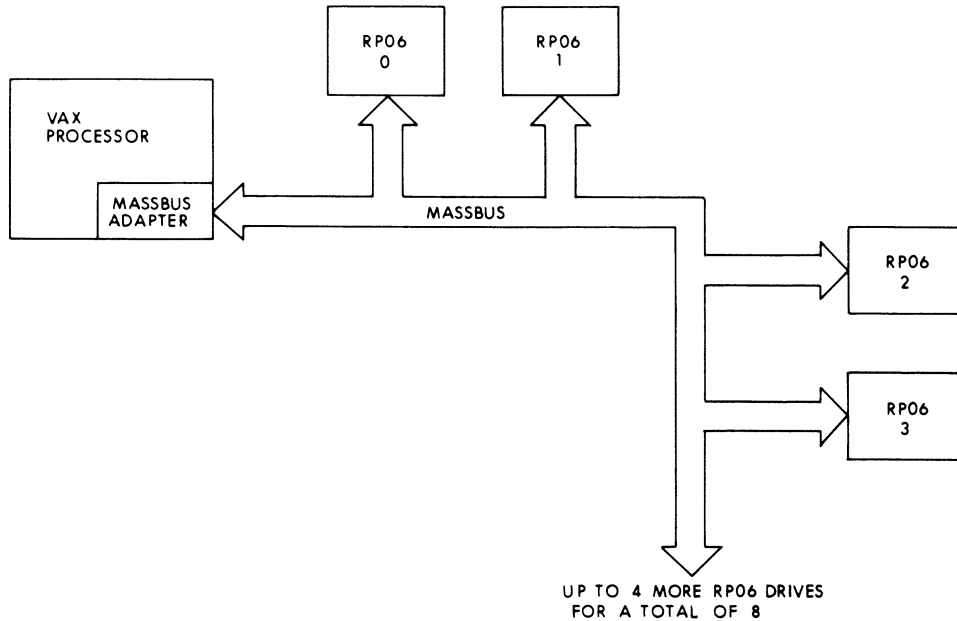


Figure 2-13 RWP06 SYSTEM BLOCK DIAGRAM



DISK DRIVES

Figure 2-14 REP06/RGP06 SYSTEM BLOCK DIAGRAM

(flux transition) in the clock area or the data area of a bit cell indicates whether the bit represented is a 1 or a 0.

### **DATA ORGANIZATION**

The RP06 disk pack consists of 10 disk platters, each recorded on both sides, enclosed between two outside platters for protection of the pack. Each disk pack contains a total of 20 surfaces: 19 data surfaces for recording and 1 servo surface permanently recorded with information used to position the read/write heads at the specified cylinder. The RP06 has 20 heads—19 are read/write heads which correspond to the 19 data surfaces and the additional head is the servo read head, which corresponds to the servo surface. The disk pack is divided into 815 cylinders. Each cylinder is divided into 19 tracks, corresponding to the 19 data surfaces. Each track is divided into 22 sectors with a data storage capacity of 4096 bits (512 bytes). Each sector is divided into a preamble, a header field and a data field. The header field consists of an 80-bit header that contains the cylinder, track, and sector addresses and an 8-bit header CRC (Cyclic Redundancy Check). The data field consists of 4096 bits (512 bytes) of data and a 16-bit data ECC (Error Correction Code). The preamble and the header field can only be written by the utility program that formats these disk packs.

### **OPERATION**

The RJP06 subsystems have 20 registers, the RWP06 subsystems have 22 registers, and the REP06 and RGP06 subsystems have 16 registers plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ or a WRITE operation can begin, the processor loads the bus address, word count, control and status 2, desired cylinder, desired sector/track address, and control and status 1 registers respectively.

The bus address register specifies the starting memory address of the location for the data to be read from or written onto the disk. The word count register specifies the number of words to be transferred between the disk and memory. The control and status 2 register selects which of the disk drives (up to 8 per controller/adaptor) is to perform the operation. The desired cylinder register and the desired sector/track address register specify the sector of the disk to be read or written.

After the bus address, word count, control and status 2, desired cylinder, and desired sector/track address registers have been loaded, the control and status 1 register is loaded with the READ or WRITE com-

mand from the processor. The command is then executed. If the heads are not currently positioned at the specified cylinder, the drive will do an implied SEEK, which moves the heads to the correct cylinder. The read/write data heads then read the headers on the specified track to locate the specified sector.

During a READ operation, data bits are read from the disk serially. The controller/adaptor assembles the bits into 16-bit parallel words and generates a parity bit for each 16-bit word. The controller/adaptor then transfers each 16-bit word plus parity to the specified memory location. This process continues until the proper word count is reached. When the READ operation has been completed, an interrupt is generated to alert the processor that the data has been read off the disk and is stored in the specified memory location.

During a WRITE operation, the controller/adaptor reads each 16-bit parallel word from the specified memory location and generates a parity bit for each. The controller/adaptor transfers each 16-bit word plus parity to the drive. The drive then serially writes the bits onto the disk. This process continues until the proper word count is reached. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RP06 ensure that the data is correct.

The RP06 uses the servo disk surface to position the read/write heads at the specified cylinder. The header field is read to verify that it is the specified cylinder, track, and sector. The header CRC is used to ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the disk. If there is a discrepancy between the two CRCs, the controller/adaptor alerts the processor by setting a bit in the error 1 register.

To ensure that data is written correctly, a WRITE CHECK command may be issued. This causes the RP06 to read the data just written and the controller/adaptor to compare it to the data stored in memory.

The ECC (Error Correction Code) logic is used to ensure that the data field has been read correctly. The data bits are used to generate a second ECC, which is then compared to the ECC read from the end of the data field on the disk. If there is a discrepancy between the two ECCs, the processor uses them to determine which bits are in error and to reconstruct the correct data. One error of up to 11 incorrect bits



in a row can be reconstructed in a sector. The controller/adaptor reports the position of the error to the processor and sends the processor an error burst pattern and an error correction pattern to allow the software to correct the error in memory. If a sector containing more than one error is reported to the processor by the controller as an uncorrectable error, the processor may invoke a suitable error recovery procedure consisting of OFFSET positioning, RECALIBRATION, and REREAD operations.

## **INTERRUPTS**

The RP06 disk system controller/adaptor uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status 1 register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the SPECIAL CONDITION or READY bit in the control and status 1 register is also set.

When the SPECIAL CONDITION bit is set, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the controller/adaptor has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 254. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RP06 disk systems provide these qualities of high reliability as well as ease of maintenance.

- Modular construction of the RP06 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Off-line diagnostic capability allows the RP06 to be serviced independent of the host processor.

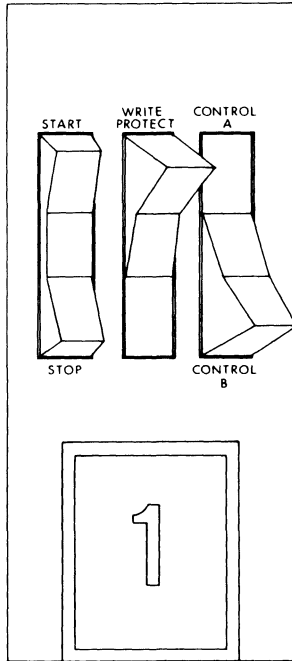


Figure 2-15 RP06 FRONT PANEL CONTROLS

### PANEL CONTROLS

The front panel controls allow the operator to control the disk drive manually. Words light up on the front panel to provide drive status information.

- START/STOP switch (2-position momentary rocker switch on front panel)

Depressing the start end of this rocker switch causes the words START and DOOR LOCKED to light on the front panel and the drive to accelerate the disk pack up to speed. Once the disk pack is up to speed, the word READY will light on the front panel.

Depressing the stop end of this rocker switch causes the words START and READY to disappear from the front panel and the drive to stop the disk pack. Once the disk pack has stopped, the words DOOR LOCKED will disappear from the front panel.

- WRITE PROTECT switch (2-position rocker switch on front panel)

When set in the write protect position, the processor is prevented from writing on the disk pack and the words WRITE PROTECT light

on the front panel. When set to the other position, WRITE operations are enabled.

- CONTROL A/CONTROL B switch (3-position rocker switch on front panel)

When set to the control A position, MASSBUS port A is enabled and the words CONTROL A light on the front panel. When set to the control B position, MASSBUS port B is enabled and the words CONTROL B light on the front panel. When set to the middle position, both MASSBUS ports are enabled. The words CONTROL A and CONTROL B light on the front panel only when accessed by the respective MASSBUS.

- DRIVE NUMBER receptacle (unlabeled receptacle on front panel)

Each drive comes with eight numbered (0-7) plugs. The drive number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, that drive cannot be selected by the processor. Note that drive number units cannot be duplicated.

## PANEL INDICATORS

Different words light on the front panel which provide drive status information to the user.

The word START lights on the front panel when the start switch has been depressed. It stays lit until the stop switch is depressed.

The words CONTROL A light on the front panel as long as the CONTROL A/CONTROL B switch is set to the control A position, enabling MASSBUS port A. The words CONTROL B light on the front panel as long as the CONTROL A/CONTROL B switch is set to the control B position, enabling MASSBUS port B. When the CONTROL A/CONTROL B switch is set to the middle position, both MASSBUS ports are enabled. The words CONTROL A and CONTROL B light on the front panel only when accessed by the respective MASSBUS.

When the word READY lights on the front panel, the disk pack is up to speed and the drive is ready to accept a command.

When the word UNSAFE lights on the front panel, the drive has detected an unsafe condition such as an internal power supply failure.

When the word STANDBY lights on the front panel, the disk pack is not up to speed and the heads are not loaded.

When the words WRITE PROTECT light on the front panel, the WRITE PROTECT switch is set to the write protect position and the drive will not accept WRITE commands.

When the words DOOR LOCKED light on the front panel, the glass door over the disk pack is locked and the disk pack may not be removed. When the words DOOR LOCKED disappear from the front panel, the glass door over the disk pack may be opened and the disk pack removed.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Freestanding
Controller/adaptor mounting code	
RJP06	2 SUs
RWP06	MASSBUS port
REP06	Option panel space
RGP06	MBA slot
Height	47 in (119 cm)
Width	33 in (83.8 cm)
Depth	32 in (81 cm)
Weight	600 lbs (273 kg)

### PERFORMANCE

Drives per controller/adaptor	8
Formatted capacity per disk pack	176 MB
Peak transfer speed	806 KB/s
Average access time*	38.3 ms
Average seek time	30 ms
Average latency (rotational) time	8.3 ms
Track-to-track seek	10 ms
Rotational speed	3600 rpm
Surfaces per disk pack	19 data, 1 servo

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

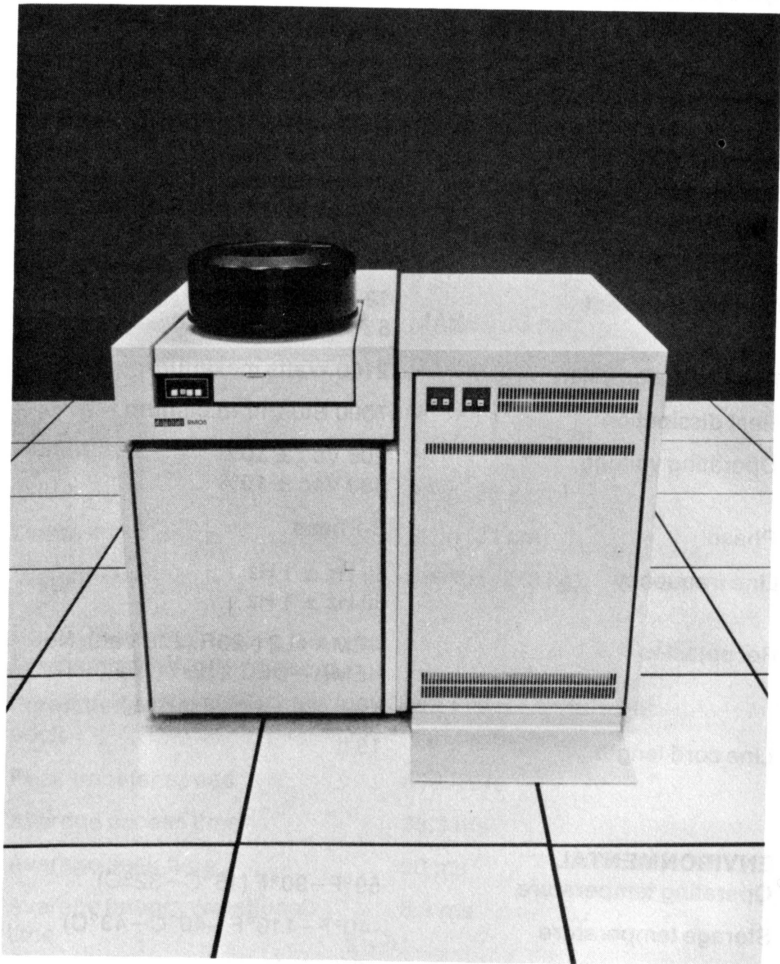
Tracks per surface	815
Sectors per track	22 (16-bit format)
Bytes per sector	512
Tracks per inch	384
Bits per inch	4040

### **ELECTRICAL**

Starting (surge) current	30 A at 208 Vac 26 A at 380 Vac
Surge duration	10 s
Operating current	12 A at 208 Vac 6 A at 380 Vac
Power Consumption	2100 Watts maximum
Heat dissipation	7000 Btus/hr maximum
Operating voltage	208 Vac $\pm$ 10% 380 Vac $\pm$ 10%
Phase	3-Phase
Line frequency	60 Hz $\pm$ 1 Hz 50 Hz $\pm$ 1 Hz
Receptacles	NEMA #L21-20R (208 Vac), Not NEMA—DEC #12-11259 (380 Vac)
Line cord length	15 ft

### **ENVIRONMENTAL**

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–110°F (-40°C–43°C)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–90% (non-condensing)
Maximum wet bulb temperature	78°F (26°C)
Maximum operating altitude	6500 ft (2000 m) above sea level



**RM05**

## **RM05**

The RM05 is a freestanding, random-access, disk storage system which connects to the processor via the MASSBUS controller/adaptor. The RWM05 subsystems are supported by PDP-11/70 systems and the REM05 subsystem are supported by VAX-11/780 systems. The RM05 was designed to operate at high speeds in high usage environments in a variety of real-time applications calling for the flexibility of off-line and on-line storage, the need for a systems interchangeable storage medium, and/or the need for off-line data security.

## **FEATURES**

- Formatted capacity of 256 MB
- Removable disk pack provides unlimited off-line storage
- Overlapped seeks optimize seek time and provide increased system throughput on multidrive systems
- Static dual-access capability
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 8 disk drives per subsystem

## **DESCRIPTION**

The RWM05-AA(AB) and REM05-AA(AB) disk storage subsystems consist of a single-access, freestanding RM05 disk drive, a utility cabinet, a drive adapter, a MASSBUS controller/adaptor, a MASSBUS cable, and a disk pack. The utility cabinet houses the drive adapter and provides space for one additional drive adapter. Up to seven more add-on RM05 drives (single-access or dual-access) may be added to these subsystems. The RM05-AA(AB) versions are single-access add-on drives with a drive adapter packaged in a utility cabinet. The RM05-AC(AD) versions are single-access add-on drives with a drive adapter but no utility cabinet. The drive adapter with the RM05-AC(AD) versions must be mounted in the available space in the utility cabinet included with the RWM05 and REM05 subsystems (single- or dual-access) or the RM05-AA(AB) and RM05-BA(BB).

The RWM05-BA(BB) and REM05-BA(BB) disk storage subsystems consist of a dual-access, freestanding RM05 disk drive, a utility cabinet, a drive adapter, two MASSBUS controllers/adapters, two MASSBUS cables, and a disk pack. The utility cabinet houses the drive adapter and provides space for one additional drive adapter. Up to seven more add-on RM05 disk drives (single-access or dual-access) may be added to these subsystems. The RM05-BA(BB) versions are dual -access add-on drives with a drive adapter packaged in a utility cabinet. The RM05-BC(BD) versions are dual-access add-on drives

with a drive adapter but no utility cabinet. The drive adapter with the RM05-BC(BD) versions must be mounted in the available space in the utility cabinet included with the RWM05 and REM05 subsystems (single- or dual-access) or the RM05-AA(AB) and RM05-BA(BB). Note that dynamic (simultaneous access) dual-port capability of disk subsystems is not supported by DIGITAL operating system software or diagnostics. However, the RWM05-BA(BB) and the REM05-BA(BB) subsystems can be statically shared by two processors or connected to one processor through two MASSBUS controllers/adapters for maximum system availability.

### **RECORDING METHOD**

The RM05 utilizes Modified Frequency Modulation (MFM) to read and write data. Data is written on the disk by magnetizing small sections (bit cells) of the oxide on the disk in different directions, i.e. either positively or negatively. A change in the direction of magnetization (flux transition) in the clock area of a bit cell indicates whether the bit represented is a 1 or a 0.

### **DATA ORGANIZATION**

The RM05 disk pack consists of 10 disk platters, each recorded on both sides, enclosed between two outside platters for protection of the pack. Each disk pack contains a total of 20 surfaces: 19 data surfaces for recording and 1 servo surface permanently recorded with information used to position the read/write heads at the specified cylinder. The RM05 has 20 heads—19 are read/write heads which correspond to the 19 data surfaces and the additional head is the servo read head, which corresponds to the servo surface. The disk pack is divided into 823 cylinders. Each cylinder is divided into 19 tracks, corresponding to the 19 data surfaces. Each track is divided into 32 sectors with a data storage capacity of 4096 bits (512 bytes). Each sector is divided into a header field and a data field. The header field consists of an 48-bit header that contains the cylinder, track, and sector addresses and a 16-bit header CRC (Cyclic Redundancy Check). The data field consists of 4096 bits (512 bytes) of data and a 32-bit data ECC (Error Correction Code). The preamble and the header field can only be written by the utility program that formats these disk packs.

### **OPERATION**

The RWM05 subsystems have 22 registers and the REM05 subsystems have 16 registers plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).



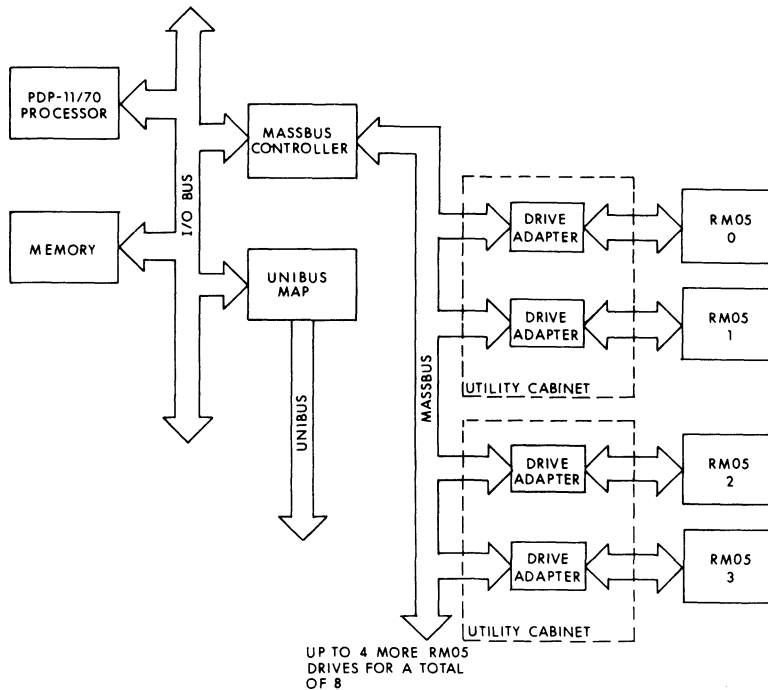


Figure 2-16 RWM05 SYSTEM BLOCK DIAGRAM

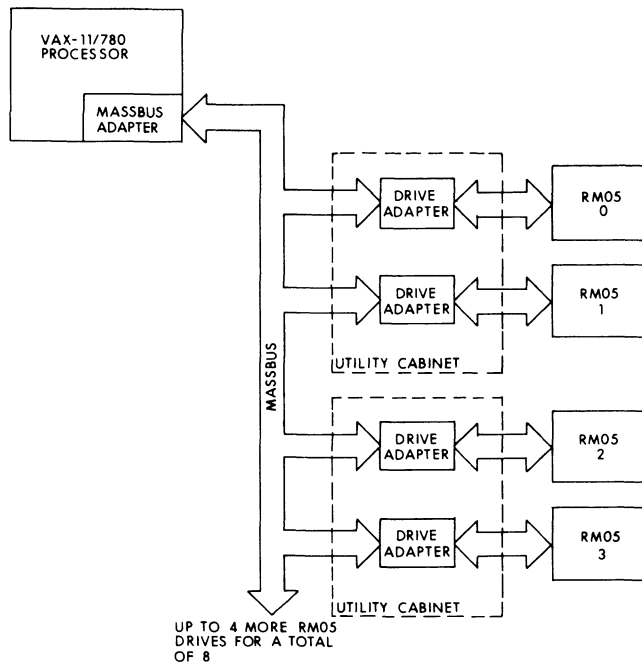


Figure 2-17 REM05 SYSTEM BLOCK DIAGRAM

Before a READ or a WRITE operation can begin, the processor loads the bus address, word count, control and status 2, desired cylinder, desired sector/track address, and control and status 1 registers respectively.

The bus address register specifies the starting memory address of the location for the data to be read from or written onto the disk. The word count register specifies the number of words to be transferred between the disk and memory. The control and status 2 register selects which of the disk drives (up to 8 per controller/adaptor) is to perform the operation. The desired cylinder register and the desired sector/track address register specify the sector of the disk to be read or written.

After the bus address, word count, control and status 2, desired cylinder, and desired sector/track address registers have been loaded, the control and status 1 register is loaded with the READ or WRITE command from the processor. The command is then executed. If the heads are not currently positioned at the specified cylinder, the drive will do an implied SEEK, which moves the heads to the correct cylinder. The read/write data heads then read the headers on the specified track to locate the specified sector.

During a READ operation, data bits are read from the disk serially. The controller/adaptor assembles the bits into 16-bit parallel words and generates a parity bit for each 16-bit word. The controller/adaptor then transfers each 16-bit word plus parity to the specified memory location. This process continues until the proper word count is reached. When the READ operation has been completed, an interrupt is generated to alert the processor that the data has been read off the disk and is stored in the specified memory location.

During a WRITE operation, the controller/adaptor reads each 16-bit parallel word from the specified memory location and generates a parity bit for each. The controller/adaptor transfers each 16-bit word plus parity to the drive. The drive then serially writes the bits onto the disk. This process continues until the proper word count is reached. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RM05 ensure that the data is correct.

The RM05 uses the servo disk surface to position the read/write heads at the specified cylinder. The sector header field is read to verify that it is the specified cylinder, track, and sector. The header CRC is used to

ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the disk. If there is a discrepancy between the two CRCs, the controller/adaptor alerts the processor by setting a bit in the error 1 register.

To ensure that data is written correctly, a WRITE CHECK command may be issued by the software. This causes the RM05 to read the data just written and the controller / adaptor to compare it to the data stored in memory.

The ECC (Error Correction Code) logic is used to ensure that the data field has been read correctly. The data bits are used to generate a second ECC, which is then compared to the ECC read from the end of the data field on the disk. If there is a discrepancy between the two ECCs, the processor uses them to determine which bits are in error and to reconstruct the correct data. One error of up to 11 incorrect bits in a row can be reconstructed in a sector. The controller/adaptor reports the position of the error to the processor and sends the processor an error burst pattern and an error correction pattern to allow the software to correct the error in memory. If a sector containing more than one error is reported to the processor by the controller/adaptor as an incorrectable error, the processor may invoke a suitable error recovery procedure consisting of OFFSET positioning, RECALIBRATION, and REREAD operations.

## **INTERRUPTS**

The RM05 disk system controller/adaptor uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status 1 register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the SPECIAL CONDITION or READY bit in the control and status 1 register is also set.

When the SPECIAL CONDITION bit is set, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the controller/adaptor has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 254. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

**RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RM05 disk systems provide them these qualities of high reliability as well as ease of maintenance.

- Modular construction of the RM05 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Off-line tester allows the RM05 to be serviced independent of the host processor.
- Easily accessible drive adapter.
- Fault-isolation diagnostics simplify troubleshooting and provide extended maintenance and serviceability.

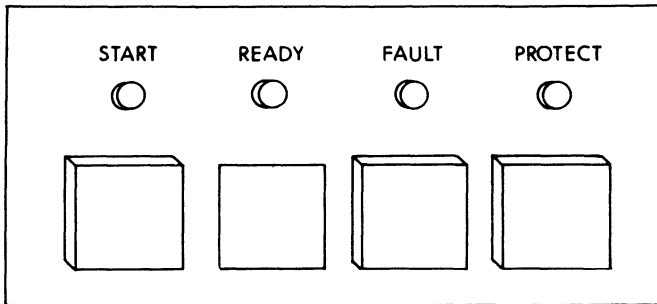
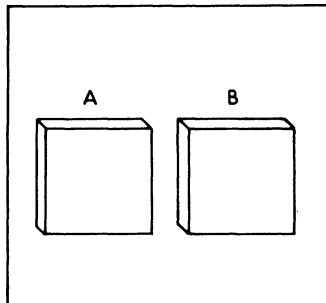
**FRONT PANEL CONTROLS AND INDICATORS****DRIVE CABINET SWITCHES**

Figure 2-18 RM05 CONTROLS AND INDICATORS

**CONTROLS AND INDICATORS**

The front panel controls allow the operator to control the disk drive manually and the indicator lights provide drive status information. The A and B switches located on the drive cabinet door allow the operator

to enable different MASSBUS ports.

- **START switch and associated lamp (alternate-action pushbutton and associated red light indicator on front panel)**

Depressing this switch causes the START indicator light to go on and the drive to accelerate the disk pack up to speed. Once the disk pack is up to speed, the READY indicator will light. Depressing the switch again causes the drive to stop the disk pack and the START indicator light to go out.

- **READY lamp (red light indicator on front panel)**

When lit, indicates that the disk pack is up to speed and the drive is ready to execute a command. This lamp will blink during start/stop sequences.

- **DRIVE NUMBER receptacle (unlabeled receptacle on front panel)**

Each drive comes with eight numbered (0-7) plugs. The drive number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, the drive cannot be selected by the processor. Note that drive number units cannot be duplicated.

- **FAULT CLEAR switch and associated lamp (momentary pushbutton and associated red light indicator on front panel)**

Depressing this switch causes the indicator light to go out if the fault condition has been corrected.

When lit, the drive has detected a hardware fault such as write current failure or a dc power supply failure.

- **WRITE PROTECT switch and associated lamp (alternate-action pushbutton and associated red light indicator on drive cabinet door)**

Depressing this switch causes the associated indicator to light and prevents the processor from writing on the disk pack. Depressing this switch again causes the indicator light to go out and enables WRITE operations.

- **A and B switches (alternate-action pushbuttons/red light indicators on drive cabinet door)**

Depressing switch A enables MASSBUS port A. Depressing switch B enables MASSBUS port B. When both switches are depressed or when neither switch is depressed, both MASSBUS ports are enabled.

The A indicator lights when the drive is being accessed by MASSBUS port A and the B indicator lights when the drive is being accessed by MASSBUS port B.

**SPECIFICATIONS**

Note that all RM05 subsystems and add-on drives are designed to run with the RM05-P disk pack.

**MECHANICAL**

Drive cabinet	Freestanding
Utility cabinet	Freestanding
Controller/adaptor mounting code	
RWM05	MASSBUS port
REM05	Option panel space
Drive height	36.2 in (91.9 cm)
Drive width	23 in (58.4 cm)
Drive depth	36 in (91.4 cm)
Drive weight	556 lbs (252.7 kg)
Utility cabinet height	36.2 in (91.9 cm)
Utility cabinet width	23 in (58.4 cm)
Utility cabinet depth	36 in (91.4 cm)
Utility cabinet weight with one drive adapter	190 lbs (86.3 kg)
Utility cabinet weight with two drive adapters	261 lbs (117.5 kg)

**PERFORMANCE**

Drives per controller/adaptor	8
Formatted capacity per disk pack	256 MB
Peak transfer speed	1200 KB/s
Average access time*	38.3 ms
Average seek time	30 ms

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

Average latency (rotational) time	8.3 ms
Track-to-track seek	6 ms
Rotational speed	3600 rpm
Surfaces per disk pack	19 data, 1 servo
Tracks per surface	823
Sectors per track	32 (16-bit format)
Bytes per sector	512
Tracks per inch	384
Bits per inch	6038

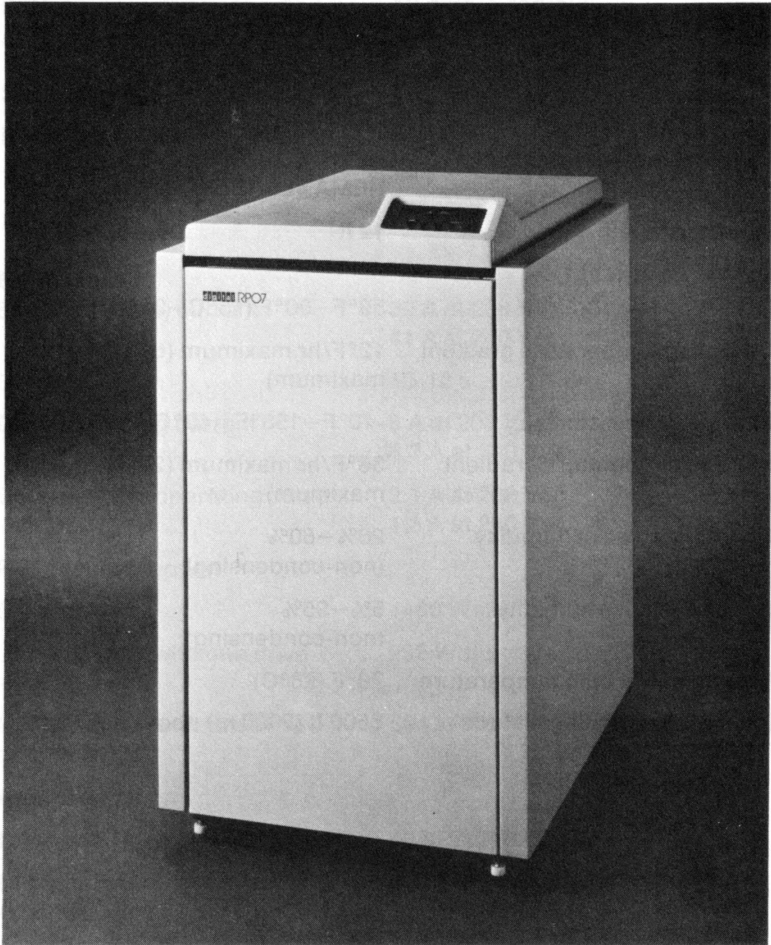
### **ELECTRICAL**

Starting (surge) current	39 A at 208 Vac 41 A at 240 Vac
Surge duration	10-12 s
Drive operating current	8 A at 208 Vac 8.7 A at 240 Vac
Drive adapter operating current	2.1 A at 208 Vac 1.3 A at 240 Vac
Power consumption	
Drive only	1460 Watts
Utility cabinet with one drive adapter	252 Watts
Utility cabinet with two drive adapters	504 Watts
Heat dissipation	
Drive only	4983 Btus/hr
Utility cabinet with one drive adapter	860 Btus/hr
Utility cabinet with two drive adapters	1720 Btus/hr
Drive operating voltage	208 Vac +14.6, -29 240 Vac +17, -27



## DISK DRIVES

Utility cabinet operating voltage	120 Vac $\pm$ 8 240 Vac +17, -27
Phase	1-phase
Line frequency	60 Hz 50 Hz
Drive receptacles	NEMA #L6-20R (208 Vac, 60 Hz), Shipped with no plug (240 Vac, 50 Hz)
Utility cabinet receptacles	NEMA #L5-15R (120 Vac), NEMA #L6-15R (240 Vac)
Line cord length	12 ft
<b>ENVIRONMENTAL</b>	
Operating temperature	59°F–90°F (15°C–32°C)
Operating temperature gradient	12°F/hr maximum (6.7°C/hr maximum)
Storage temperature	-40°F–158°F (-40°C–70°C)
Storage temperature gradient	36°F/hr maximum (20°C/hr maximum)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	78°F (26°C)
Maximum operating altitude	6500 ft (2000 m) above sea level



**RP07**

## **RP07**

The RP07 is a freestanding, random-access, disk storage system which connects to the processor via the MASSBUS adapter (MBA). The REP07 subsystems are supported by VAX-11/780 systems only. The RP07 was designed to operate at very high speeds in high usage environments in a wide range of real-time applications, requiring high capacity for low cost, high capacity for the smallest floorspace, and the inherent high reliability of Winchester technology.

## **FEATURES**

- Formatted capacity of 516 MB
- Winchester fixed-media technology
- Sealed Head Disk Assembly (HDA)
- Internal microprocessor-controlled diagnostics
- Overlapped seeks optimize seek time and provide increased system throughput on multidrive systems
- Static dual-access capability
- Direct Memory Access (DMA) data transfers
- Expandable up to a total of 8 disk drives per subsystem

## **DESCRIPTION**

The REP07-AB(AD) disk storage subsystems consist of a single-access, freestanding RP07 disk drive with non-removable head disk assembly, a MASSBUS adapter (MBA), and a MASSBUS cable. Up to seven more add-on RP07 disk drives (single- or dual-access) may be added to these subsystems.

The REP07-BA(BB) disk storage subsystems consist of a dual-access, freestanding RP07 disk drive with non-removable head disk assembly, two MASSBUS adapters (MBAs), and two MASSBUS cables. Up to seven more add-on RP07 disk drives (single- or dual-access) may be added to these subsystems. Note that dynamic (simultaneous access) dual-port capability of disk subsystems is not supported by DIGITAL operating system software or diagnostics. However, the REP07-BA(BB) subsystems can be statically shared by two processors or connected to one processor through two MBAs for maximum system availability.

## **DATA ORGANIZATION**

The RP07 head disk assembly consists of 9 disk platters, each recorded on both sides except the top one. Each head disk assembly contains a total of 17 surfaces: 16 data surfaces for recording and 1 servo surface permanently recorded with information used to position the read/write heads at the specified cylinder. The RP07 has 33

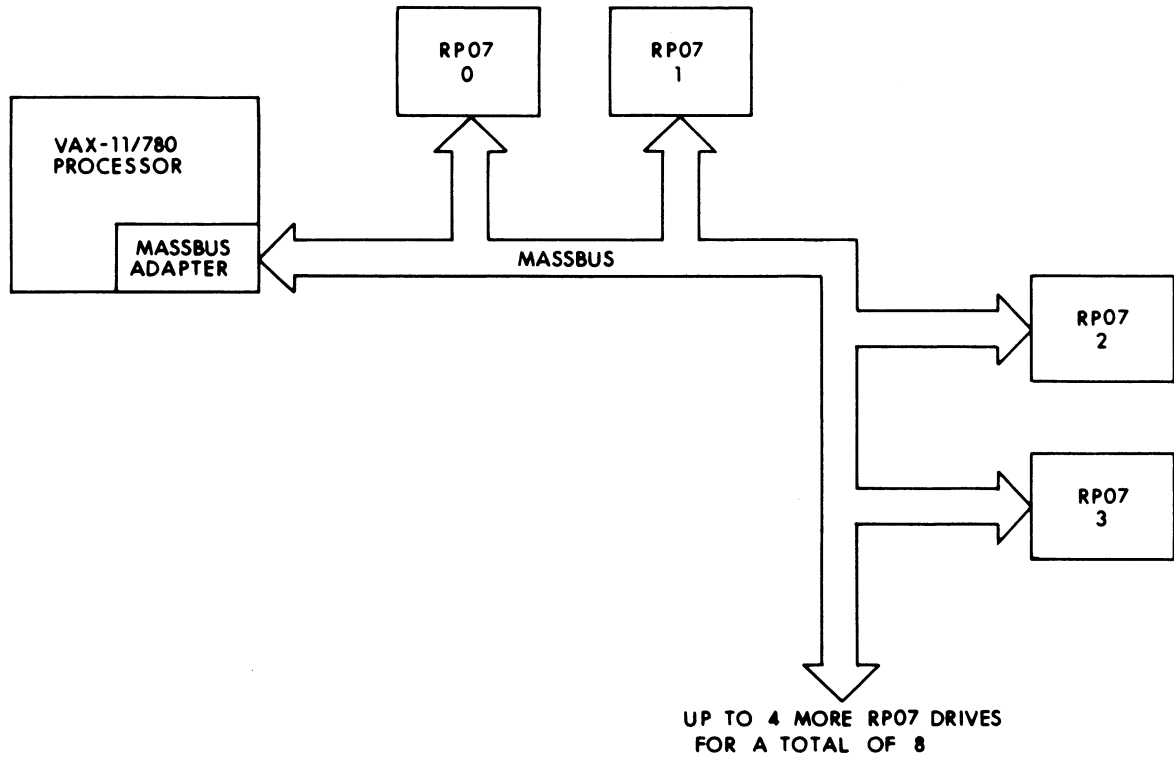


Figure 2-19 REP07 SYSTEM BLOCK DIAGRAM

heads—32 are read/write heads (two per data surface) and the additional head is the servo read head, which corresponds to the servo surface. The head disk assembly is divided into 632 cylinders: 630 are used for data and 2 are used for diagnostics. Each cylinder is divided into 32 tracks (two per data surface). Each track is divided into 50 sectors with a data storage capacity of 4096 bits (512 bytes). At the beginning of each track is a 128-bit track descriptor field which contains the track and cylinder addresses, media defect information, and the CRC words. Each sector is divided into a header field and a data field. The header field consists of a 128-bit header that contains the cylinder, track, and sector addresses and a 32-bit header CRC (Cyclic Redundancy Check). The data field consists of 4096 bits (512 bytes) of data and a 32-bit data ECC (Error Correction Code). The track descriptor and the header field can only be written by the utility program that formats these head disk assemblies.

## **OPERATION**

The REP07 has sixteen registers plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ or WRITE operation can begin, the processor loads the MBA virtual address, MBA byte counter, desired cylinder, desired track/sector address, and control and status 1 registers respectively.

The MBA virtual address register specifies the starting memory address of the storage location for the data to be read from or written onto the disk. The MBA byte counter register specifies the total number of bytes to be transferred between the disk and memory. The desired cylinder register and the desired track/sector address register specify the sector of the disk to be read or written.

After the MBA virtual address, MBA byte counter, desired cylinder, and desired track/sector address registers have been loaded, the control and status 1 register is loaded with the READ or WRITE command from the processor. The command is then executed. If the heads are not currently positioned at the specified cylinder, the drive will do an implied SEEK, which moves the heads to the correct cylinder. The read/write heads then read the headers on the specified track to locate the specified sector. If an index marker is found prior to the target sector, the RP07 will reorient the search for the target sector relative to the index marker.

During a READ operation, data bits serially read off the disk are assembled into 16-bit parallel words and a parity bit is generated for each 16-bit word. Every 16-bit word plus parity is then transferred to

the MBA. The MBA combines two 16-bit words into a 32-bit memory word and generates a parity bit for each 32-bit word. Every 32-bit word plus parity is then transferred to the memory location specified. This process continues until the byte count in the MBA virtual address register is reached. When the READ operation is completed, an interrupt is set to alert the processor that the data has been read off the disk and stored in the specified memory location.

During a WRITE operation, each 32-bit word of data is read from memory and transferred to the MBA which divides the 32-bit word into two 16-bit parallel words and generates a parity bit for each 16-bit word. The MBA then transfers the two 16-bit words plus parity to the drive. The drive checks the parity and then serially writes the bits onto the disk. This process continues until the proper word count is reached. When the WRITE operation has been completed, an interrupt is generated to alert the processor that the data has been written onto the disk.

### **DATA INTEGRITY**

Several error checking and correction features of the RP07 ensure that the data is correct.

The RP07 uses the servo disk surface to position the read/write heads at the specified cylinder. The sector header field is read to verify that it is the specified cylinder, track, and sector. The header CRC is used to ensure that the header field has been read correctly. The header bits are used to generate a second CRC, which is then compared to the CRC read from the end of the header field on the disk. If there is a discrepancy between the two CRCs, the MBA alerts the processor by setting HEADER CRC ERROR <08> in the error 1 register.

To ensure that data is written correctly, a WRITE CHECK command may be issued by the software. This causes the RP07 to read the data just written and the MBA to compare it to the data stored in memory.

The ECC (Error Correction Code) logic is used to ensure that the data field has been read correctly. The data bits are used to generate a second ECC, which is then compared to the ECC read from the end of the data field on the disk. If there is a discrepancy between the two ECCs, the processor uses them to determine which bits are in error and to reconstruct the correct data. One error of up to 11 incorrect bits in a row can be reconstructed in a sector. The MBA reports the position of the error to the processor and sends the processor an error burst pattern and an error correction pattern to allow the software to correct the error in memory. If a sector contains more than one error, the MBA alerts the processor by setting ECC HARD ERROR <06> in the error 1 register.

**INTERRUPTS**

The RP07 disk system MBA uses a vectored interrupt to cause the program to branch to an interrupt service routine. The RP07 generates an interrupt at the completion of an operation, when a error has been detected, or when a drive comes on-line.

**RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the disk system. Special design features of the RP07 disk systems provide these qualities of high reliability as well as ease of maintenance.

- Winchester technology (Sealed Head Disk Assembly) requires no alignment of the heads.
- Easy front access to most assemblies.
- Modular construction of the RP07 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Integral maintenance keypad and display allow for microprocessor-controlled diagnostics to be performed independent of the host processor.
- On-line microprocessor-controlled diagnostic capability alerts the host processor to microprocessor failure.

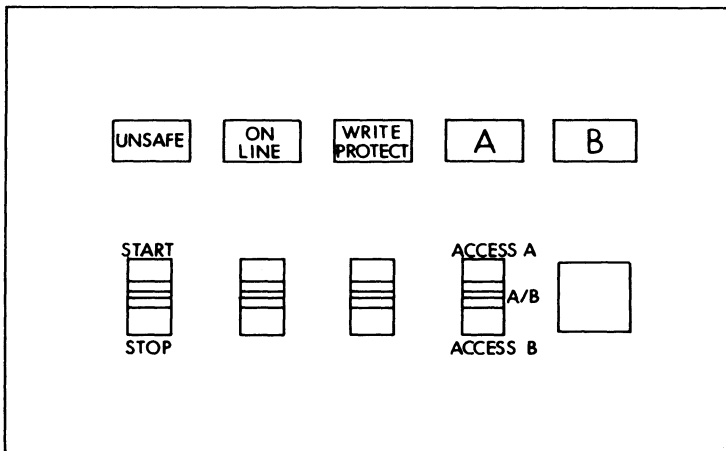


Figure 2-20 RP07 FRONT PANEL CONTROLS

## **PANEL CONTROLS AND INDICATORS**

The front panel controls allow the operator to control the disk drive manually. The indicator lights provide drive status information.

- **START/STOP switch (2-position toggle switch on front panel)**

When set to the start position, causes the drive to accelerate the head disk assembly up to speed. When set to the stop position, causes the drive to stop the head disk assembly.
- **ON-LINE switch (2-position toggle switch below the ON-LINE indicator on front panel)**

When set to the up position, makes the drive available to the processor. When set to the down position, makes the drive unavailable to the processor.
- **WRITE PROTECT switch (2-position toggle switch below the WRITE PROTECT indicator on front panel)**

When set to the up position, causes the WRITE PROTECT indicator to light and prevents the processor from writing on the head disk assembly. When set to the down position, causes the WRITE PROTECT indicator light to go out and enables WRITE operations.
- **ACCESS A, A/B, ACCESS B switch (3-position toggle switch on front panel)**

When set to the access A position, MASSBUS port A is enabled. When set to the access B position, MASSBUS port B is enabled. When set to the A/B position, both MASSBUS ports are enabled.
- **UNSAFE indicator (yellow light indicator on front panel)**

When lit, indicates that the drive has detected an unsafe condition such as a start-spindle error. When blinking, indicates that the drive has detected an early temperature warning or an inadequate air flow.
- **ON-LINE indicator (yellow light indicator on front panel)**

When lit, indicates that the drive is available to the processor. The ON-LINE indicator light goes out when the ON-LINE switch is set to the down position, the START/STOP switch is set to the stop position, or the UNSAFE indicator lights.
- **WRITE PROTECT indicator (yellow light indicator on front panel)**

The WRITE PROTECT indicator lights when the WRITE PROTECT switch is set to the up position and goes out when the WRITE PROTECT switch is set to the down position.



## DISK DRIVES

- A indicator (yellow light indicator on front panel)  
The A indicator lights when the drive is being accessed by MASS-BUS port A.
- B indicator (yellow light indicator on front panel)  
The B indicator lights when the drive is being accessed by MASSBUS port B.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Freestanding
Controller mounting code (REP07)	Option panel space
Height	46.5 in (118.1 cm)
Width	26.5 in (67.3 cm)
Depth	33 in (83.8 cm)
Weight	400 lbs (181 kg)

### PERFORMANCE

Drives per controller	8
Formatted capacity per head disk assembly	516 MB
Peak transfer speed	1300 KB/s 2200 KB/s (with RP07-D option)
Average access time*	31.3 ms
Average seek time	23 ms
Average latency (rotational) time	8.3 ms
Track-to-track seek	5 ms
Rotational speed	3633 rpm
Surfaces per head disk assembly	16 data, 1 servo

\* Average access time is defined as the sum of the average seek time and the average latency (rotational) time.

## DISK DRIVES

Tracks per surface	1260 data +4 for diagnostic testing
Sectors per track	50 (16-bit format)
Bytes per sector	512
Tracks per inch	537
Bits per inch	11,139

### **ELECTRICAL**

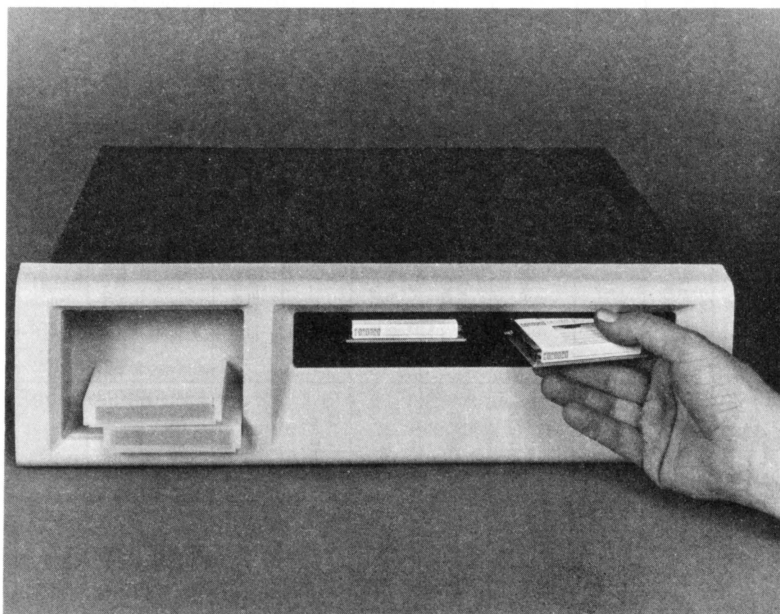
Starting (surge) current	70 A
Surge duration	4 s
Operating current	8 A
Power Consumption	2000 Watts
Heat dissipation	7000 Btus/hr
Operating voltage	208 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	3-Phase
Line frequency	60 Hz $\pm$ 1 Hz 50 Hz $\pm$ 1 Hz
Receptacles	NEMA #L21-20R (208 Vac), Shipped with no plug (240 Vac)
Line cord length	15 ft

### **ENVIRONMENTAL**

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Temperature gradient	25°F/hr (-4°C/hr)
Operating relative humidity	20%–80% (non-condensing)
Maximum wet bulb temperature	78°F (26°C)
Storage relative humidity	5%–90% (non-condensing)
Maximum operating altitude	8000 ft (2400 m) above sea level

## DISK DRIVES

	RX02	RL01/RL02	RK07	RM02/RM03	RM80	RP06	RM05	RP07
<b>MEDIA TYPE</b>	FRONTLOADING DISKETTE	TOPLOADING CARTRIDGE	TOPLOADING CARTRIDGE	REMOVABLE DISK PACK	HEAD DISK ASSEMBLY	REMOVABLE DISK PACK	REMOVABLE DISK PACK	HEAD DISK ASSEMBLY
<b>DRIVES PER CONTROLLER</b>	2	4	8	8	8	8	8	8
<b>FORMATTED CAPACITY</b>	1.0MB PER DUAL-DRIVE SUBSYSTEM	RL01: 5.2 MB RL02: 10.4 MB PER DISK CARTRIDGE	28 MB PER DISK CARTRIDGE	67 MB PER DISK PACK	124 MB PER DISK PACK	176 MB PER DISK PACK	256 MB PER DISK PACK	516 MB PER DISK PACK
<b>PEAK TRANSFER SPEED</b>	61KB/S	512 KB/S	538KB/S	RM02: 806KB/S RM03: 1200KB/S	1200-KB/S	806KB/S	1200KB/S	1300KB/S 2200KB/S (with RP07-D)
<b>AVERAGE ACCESS TIME</b>	262 ms	67.5 ms	49 ms	RM02: 42.5 ms RM03: 38.3 ms	33.3 ms	38.3 ms	38.3 ms	31.3 ms
<b>AVERAGE SEEK TIME</b>	154 ms	55 ms	36.5 ms	30 ms	25 ms	30 ms	30 ms	23 ms
<b>AVERAGE LATENCY TIME</b>	83 ms	12.5 ms	12.5 ms	RM02: 12.5 ms RM03: 8.3 ms	8.3 ms	8.3 ms	8.3 ms	8.3 ms
<b>TRACK-TO-TRACK SEEK</b>	6 ms	15 ms	6.5 ms	6 ms	6 ms	10 ms	6 ms	5 ms
<b>ROTATIONAL SPEED</b>	360 rpm	2400 rpm	2400 rpm	RM02: 2400 rpm RM03: 3600 rpm	3600 rpm	3600 rpm	3600 rpm	3633 rpm
<b>DUAL-ACCESS OPTION</b>	NO	NO	YES	YES	YES	YES	YES	YES



**TU58**

## CHAPTER 3

# CARTRIDGE/MAGNETIC TAPES

### TU58

The TU58 is a 2-track, dual-drive, cartridge tape system connected to the UNIBUS via the controller. The TU58 is supported by UNIBUS PDP-11 systems with a DL11-E or DL11-W. Its low cost makes it ideal for inexpensive archive mass storage or as a diagnostic load device or software update distribution medium.

### FEATURES

- Complete cartridge tape subsystem in a compact package
- Convenient pocket-sized tape cartridge
- Automatic soft-error recovery via read retries
- Internal microprocessor diagnostics
- Data interchange with other operating systems
- Random access data format

### DESCRIPTION

The TU58 tape subsystem includes two cartridge tape transports, a controller, one 18 ft (5.5 m) I/O cable to interface to the PDP-11 UNIBUS via a DL11-E or DL11-W serial line interface (the serial line interface is not included), a universal power supply with both 120 Vac and 240 Vac power cords, and two TU58-K tape cartridges, for a total of 512 KB mass storage. Each controller will support two cartridge transports although only one may operate at a time. PDP-11 systems will support up to two TU58 subsystems for a total of 4 cartridge transports. The TU58-DA version is cabinet-mountable and comes with the necessary hardware for mounting in standard cabinetry while the TU58-EB version is a self-contained tabletop unit. The TU58 reads and writes data at 800 b/in at a tape speed of 30 in/s.

The TU58 is connected to the processor via the UNIBUS by a single-line, asynchronous DL11-E or DL11-W interface (not included). The TU58 data transfer speed is jumper-selectable from 150 to 38,400 baud. Note that the maximum data transfer speed for the DL11-E and the DL11-W is 9600 baud.

The data interchange capability of the TU58 allows the user to write files using one operating system and to read them back using another operating system.

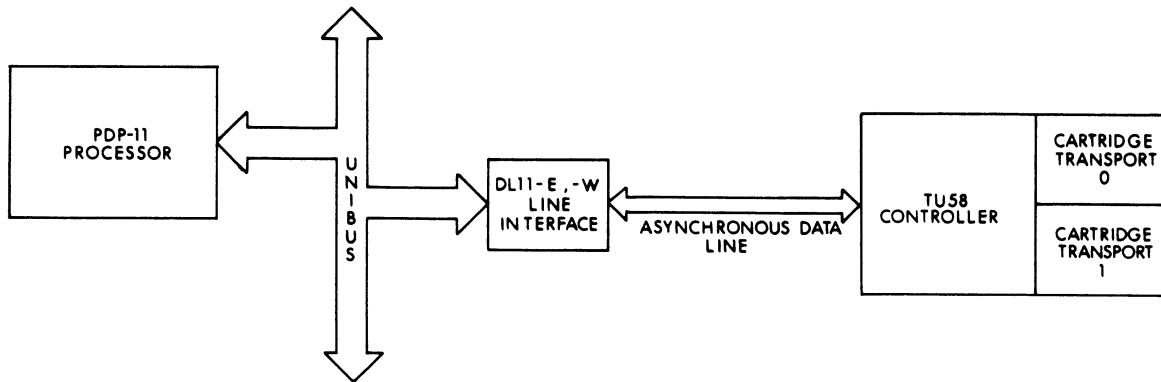


Figure 3-1 TU58 SYSTEM BLOCK DIAGRAM

## OPERATION

The TU58 is accessed through the DL11-E or DL11-W serial line interface. When used with the TU58, the DL11-E and the DL11-W use the following four registers: the Receiver Status Register, the Receiver Data Buffer Register, the Transmitter Status Register, and the Transmitted Data Buffer Register. (Refer to the register section at the back of this book for applicable register diagrams and bit definitions.)

The TU58 accesses data randomly since the data is stored at fixed locations (blocks of 512 bytes each) on the tape rather than at unknown or variable locations. Replacement of data blocks on the tape is random and does not interfere with data blocks recorded previously. During a READ operation, the TU58 reads the format information already on the tape and uses it to locate data to be read off the tape. During a WRITE operation, the same format information is used by the TU58 to locate the block where the data is to be written onto the tape.

Data is written on the tape in two tracks. Both tracks are used for reading and writing forward.

The TU58 microprocessor controller includes a 2 KB ROM and a 256 byte RAM. 128 bytes of the RAM are used as a scratchpad by the microprogram and the other 128 bytes are used to buffer the data sent to or from the processor.

Commands and data are sent to and from the TU58 in groups of bytes called message packets using the Radial Serial Protocol (RSP) format. There are six types of message packets: COMMAND, DATA, CONTINUE, XOFF, INITIALIZE, and BOOTSTRAP.

Before a READ operation can begin, the processor sends the TU58 microprocessor controller a COMMAND packet. The COMMAND packet selects which of the available transports (up to 2 per controller) is to perform the READ operation, specifies the starting address of the block to be read, and specifies the number of bytes to be read (byte count). The TU58 then positions the tape and starts reading data from the block specified by the controller. The TU58 reads the first 128 bytes of data off the tape and stores them in the RAM data buffer. The controller then sends the 128 bytes of data to the processor via the DL11-E or DL11-W. The TU58 will continue to read sequential blocks of data in 128 byte increments until the byte count specified by the processor has been reached. After the specified byte count has been reached, the controller sends an END packet to the processor. The END packet tells the processor that the specified number of bytes have been read and lists any error messages.

## MAGNETIC TAPES

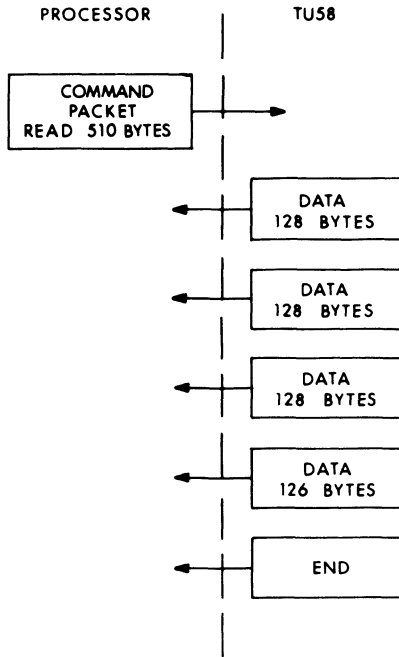


Figure 3-2 READ Command Sequence

Before a WRITE operation can begin, the processor also sends the TU58 microprocessor controller a COMMAND packet. The COMMAND packet selects which of the available transports (up to 2 per controller) is to perform the WRITE operation, specifies the starting address of the block to be written, and specifies the number of bytes to be written (byte count). The TU58 receives the first 128 bytes of data from the processor via the DL11-E or DL11-W and stores them in the RAM data buffer. The controller then writes the 128 bytes of data on the tape. If the specified byte count has not yet been reached, the TU58 controller will send a CONTINUE packet to the processor. The CONTINUE packet tells the processor to send the next 128 bytes of data to be written on the tape. The TU58 will continue to write sequential blocks of data in 128 byte increments until the byte count specified by the processor has been reached. After the specified byte count has been reached, the controller sends an END packet to the processor. The END packet tells the processor that the specified number of bytes have been written and lists any error messages.



# MAGNETIC TAPES

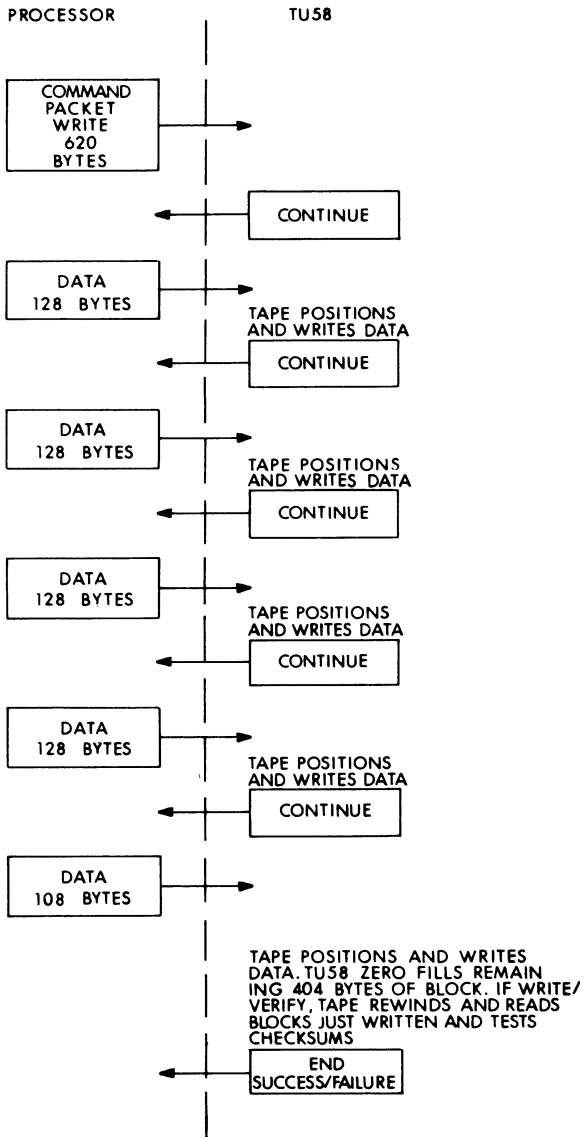


Figure 3-3 WRITE Command Sequence

The six types of message packets are: COMMAND, DATA, CONTINUE, XOFF, INITIALIZE, and BOOTSTRAP. The message packet structures are defined below.

### COMMAND PACKET

The COMMAND message packet contains fourteen bytes and is used by the processor to initiate a READ, WRITE, or POSITION operation, to obtain status information from the microprocessor controller, or to cause the controller to perform self-diagnostics. The COMMAND packet structure is as follows:

Byte 0	002 <sub>8</sub>	Flag byte indicating that this is a COMMAND packet.
Byte 1	012 <sub>8</sub>	Packet byte count.
Byte 2		Operation code.
	000 <sub>8</sub>	NO OPERATION  Causes the TU58 to return an END packet.
	001 <sub>8</sub>	RESET  Causes the TU58 to initialize and return an END packet.
	002 <sub>8</sub>	READ or READ WITH INCREASED THRESHOLD  Causes the TU58 to read the specified number of bytes starting at the specified block. If bit <0> in byte 3 is set, the READ operation is performed with the threshold increased. This causes the READ operation to fail if the data on the tape is weak.
	003 <sub>8</sub>	WRITE or WRITE AND VERIFY  Causes the TU58 to write the specified number of bytes starting at

the specified block. The controller loads any remaining bytes in the last block with zeros. If bit <0> in byte 3 is set, the TU58 writes the data, backs the tape up, and then reads the data with the threshold increased and tests the checksum of each 128 byte record.

005<sub>8</sub>

POSITION

Causes the TU58 to move the tape to the specified block and then return an END packet.

007<sub>8</sub>

DIAGNOSE

Causes the TU58 to run its internal diagnostic program to test the microprocessor, ROM, and RAM and then return an END packet.

010<sub>8</sub>

GET STATUS

Causes the TU58 to return an END packet.

011<sub>8</sub>

SET STATUS

Causes the TU58 to return an END packet.

100<sub>8</sub>

END packet

Refer to END packet description.

Byte 3

000<sub>8</sub>

Modifier

Refer to READ and WRITE operation codes (byte 2). Bit 7 sets Special Address Mode. The TU58 will address the tape as 2048 blocks (0–2047) each containing 128

		bytes instead of the normal 512 blocks (0–511) each containing 512 bytes.
Byte 4		Transport number  Selects transport 0 or 1.
Byte 5		Switches  Setting bit 4 inhibits read command retries (Maintenance mode).
Bytes 6,7	000 <sub>8</sub>	These bytes are always zero.
Bytes 8,9		Byte count.  Number of bytes to be transferred by a READ or WRITE operation (0-511).
Bytes 10,11		Block number.  Starting block number for READ and WRITE operations (0-511).
Bytes 12,13		Checksum of bytes 0-11.

**END PACKET**

The END message packet, essentially a type of COMMAND packet, contains fourteen bytes and is used by the microprocessor controller to signal the end of an operation to the processor and to send error messages, if appropriate. The END packet structure is as follows:

Byte 0	002 <sub>8</sub>	Flag byte indicating that this is a COMMAND packet.
Byte 1	012 <sub>8</sub>	Packet byte count.
Byte 2	100 <sub>8</sub>	END packet operation code.

MAGNETIC TAPES

Byte 3		Success code
	000 <sub>8</sub>	0 <sub>10</sub> Normal success.
	001 <sub>8</sub>	1 <sub>10</sub> Success but with retries.
	377 <sub>8</sub>	-1 <sub>10</sub> Failed self-test.
	376 <sub>8</sub>	-2 <sub>10</sub> Partial operation (end of tape).
	370 <sub>8</sub>	-8 <sub>10</sub> Non-existent transport number.
	367 <sub>8</sub>	-9 <sub>10</sub> No cartridge.
	365 <sub>8</sub>	-11 <sub>10</sub> Write protected.
	357 <sub>8</sub>	-17 <sub>10</sub> Data error.
	340 <sub>8</sub>	-32 <sub>10</sub> Seek error (block not found).
	337 <sub>8</sub>	-33 <sub>10</sub> Motor stopped.
	320 <sub>8</sub>	-48 <sub>10</sub> Invalid operation code.
	311 <sub>8</sub>	-55 <sub>10</sub> Invalid block number (greater than 511 <sub>10</sub> ).
Byte 4		Transport number
		Transport 0 or 1.
Bytes 5-7	000 <sub>8</sub>	Not used.
Bytes 8-9		Byte count
		Number of bytes transferred.
Byte 10	000 <sub>8</sub>	Not used.

Byte 11	Status summary
	Bit 4, Logic error.
	Bit 5, Motion error.
	Bit 6, Transfer error.
	Bit 7, Special Condition. Indicates that one of the other error bits <4-6> is set.
Bytes 12,13	Checksum of bytes 0–11.

**DATA PACKET**

The DATA message packet contains up to 131 bytes (128 bytes of data) and is used by the processor to transfer data during a WRITE operation and by the microprocessor controller to transfer data during a READ operation. The DATA packet structure is as follows:

Byte 0	001 <sub>8</sub>	Flag byte indicating that this is a DATA packet.
Byte 1	n	Byte count (up to 128 <sub>10</sub> ).
Byte 2	Data	First data byte.
	.	
	.	
	.	
Byte n	Data	
Byte n+1	Data	Last data byte.
Byte n+2		Checksum low-byte.
Byte n+3		Checksum high-byte.

**CONTINUE PACKET**

The CONTINUE message packet contains one byte and is used by the microprocessor controller during a WRITE operation to request additional data from the processor or in response to a BREAK signal from the processor. The CONTINUE packet structure is as follows:

Byte 0	020 <sub>8</sub>	Flag byte indicating that this is a CONTINUE packet.
--------	------------------	--

Returned by the TU58 to indicate that it is ready for the next data packet. Also returned in response to a BREAK signal, bit <0> of the transmitter status register.

**XOFF PACKET**

The XOFF message packet contains one byte and is used by the microprocessor controller during a READ operation to temporarily stop data transfers. The XOFF packet structure is as follows:

Byte 0	023 <sub>8</sub>	Flag byte indicating that this is a XOFF packet.
--------	------------------	--

When the processor sends XOFF, the TU58 stops sending data within two bytes until it receives a CONTINUE packet from the processor.

**INITIALIZE PACKET**

The INITIALIZE message packet contains one byte and is used by the processor to initialize the microprocessor controller and by the controller to signal that it has been turned on or that it has detected a protocol error. The INITIALIZE packet structure is as follows:

Byte 0	004 <sub>8</sub>	Flag byte indicating that this is an INITIALIZE packet.
--------	------------------	---

When sent to the TU58, causes it to reinitialize and return a CONTINUE packet. When the TU58 detects a protocol error it returns INITIALIZE packets continuously until the

processor sends a BREAK signal, bit <0> of the transmitter status register. The TU58 then returns a CONTINUE packet. When the TU58 is turned on, it returns INITIALIZE packets continuously. The processor sends a BREAK signal and two INITIALIZE packets. The TU58 will then return a CONTINUE packet.

### BOOTSTRAP PACKET

The BOOTSTRAP message packet contains two bytes and is used to boot the PDP-11 operating system. The BOOTSTRAP packet structure is as follows:

Byte 0	010 <sub>8</sub>	Flag byte indicating that this is a BOOTSTRAP packet.
Byte 1		Selects transport 0 or 1.

When sent to the TU58, causes it to position the tape at block 0 and to return 512 bytes of data without any RSP format bytes.

### DATA INTEGRITY

The TU58 controller uses a checksum character (16-bit error checking word) to ensure accurate data recording and retrieval. During a WRITE operation, the checksum character is generated and written on the tape at the end of each 128 byte record. During a READ operation, the data read is used to generate a second checksum character which is then compared to the checksum read from the end of the record. If an error is found, the controller automatically retries the READ operation. If it is unsuccessful after eight retries, the controller signals the error to the processor via the END packet.

The TU58 tape cartridge has a file-protect tab which prevents accidental writing on the tape. To write on the tape cartridge, the tab should be set to the outer position. When the tab is set to the inner position, the tape cartridge cannot be written on.



## **INTERRUPTS**

The TU58 system controller uses vectored interrupts to cause the program to branch to interrupt service routines.

An interrupt can occur during a READ operation only if the RECEIVER INTERRUPT ENABLE bit in the receiver status register is set. Once this bit is set, an interrupt request is generated after the TU58 has read one byte of data off the tape or whenever the ERROR bit in the receiver data buffer register is set. When the ERROR bit is set, it indicates that some error condition exists (the ERROR bit is set by either the OVER-RUN or BREAK bits in the receiver status register) and an interrupt is generated to cause the program to branch to an error handling routine.

An interrupt can occur during a WRITE operation only if the TRANSMITTER INTERRUPT ENABLE bit in the transmitter status register is set. The TU58 interrupts the processor after it has written one byte of data onto the tape to request an additional byte of data.

The TU58, via the DL11-E or DL11-W serial line interface, uses floating interrupt vector address assignments. The interrupt priority level is 4. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy, data integrity, and uninterrupted processing of the cartridge tape system. Special design features of the TU58 cartridge tape systems give them these qualities of high reliability as well as ease of maintenance.

- The simple, single-point drive mechanism minimizes possible damage to the tape, thereby increasing cartridge life span.
- Modular construction of the TU58 enables parts to be quickly removed and replaced during routine servicing and maintenance.

## **SPECIFICATIONS**

### **MECHANICAL**

Cabinet

TU58-DA 5.25 in (13.3 cm) panel space

TU58-EB Tabletop

## MAGNETIC TAPES

Interface (DL11-E, -W) mounting code	One quad slot
Height	5.25 in (13.3 cm)
Width	19 in (48.3 cm)
Depth	17 in (38.1 cm)
Weight	20 lbs (9 kg)

### PERFORMANCE

Cartridge transports per controller	2 (only one may operate at a time)
Recording density	800 b/in
Read/write speed	30 in/s
Capacity per cartridge	262 KB (formatted in 512 blocks of 512 bytes each)
Data transfer speed	3.7 KB/s (38.4 Kbaud) maximum
Average access time	9.3 s
Maximum access time	28 s
Flux reversal density	2400 fr/in (945 fr/cm)

### ELECTRICAL

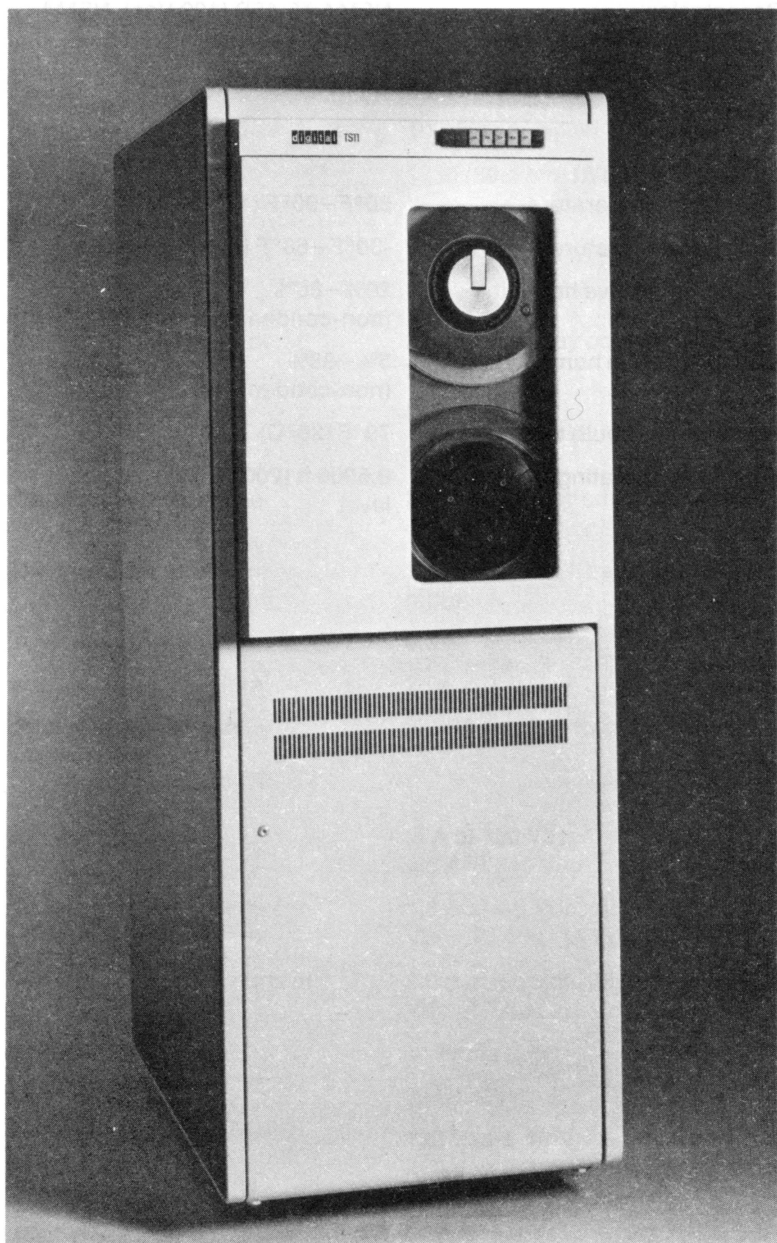
Operating current	.5 A at 120 Vac .25 A at 240 Vac
Interface (DL11-E) current	1.8 A at +5 Vdc, .05 A at +15 Vdc, .15 A at -15 Vdc
Interface (DL11-W) current	2.0 A at +5 Vdc, .05 A at +15 Vdc, .15 A at -15 Vdc
Power consumption	11 Watts
Heat dissipation	38 Btus/hr
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	60 Hz $\pm$ 3 Hz 50 Hz $\pm$ 3 Hz

## MAGNETIC TAPES

Receptacles	NEMA #5-15R (120 Vac), NEMA #6-15R (240 Vac)
Line cord length	6 ft (2 m)

### **ENVIRONMENTAL**

Operating temperature	50°F–90°F (10°C–32°C)
Storage temperature	-30°F–60°F (-34°C–50°C)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–98% (non-condensing)
Maximum wet bulb temperature	79°F (26°C)
Maximum operating altitude	6,500 ft (2000 m) above sea level



**TS11**

## **TS11**

The TS11 is a 9-track, freestanding, tape storage system which connects to the UNIBUS via the interface/controller. The TS11 subsystems are supported by UNIBUS PDP-11 and VAX-11 systems and comes in three complementary cabinet styles. The TS11 was designed to operate at medium speeds in moderate usage environments in a variety of applications, such as disk-to-tape backup for small to medium disks, software distribution medium, and tape interchange.

## **FEATURES**

- Recording density at 1600 b/in (PE)
- Read/write speed of 45 in/s
- Integral microprocessor for transport control and self-test
- Direct Memory Access (DMA) data transfers
- Quiet operation due to tension arm tape buffering

## **DESCRIPTION**

The TS11 magnetic tape storage subsystems consist of a freestanding tape transport, a microprocessor-controlled formatter and its power supply mounted in the transport cabinet, a UNIBUS interface/controller, and an I/O cable. The TS11-BA(BB) versions are configured in H9602 cabinets and are compatible with UNIBUS PDP-11 and VAX-11/780 systems. The TS11-CA(CB) versions are configured in H9646 cabinets and are compatible with PDP-11/24, PDP-11/44, and VAX-11/750 systems. TS11-DA(DB) versions are configured in H960 cabinets and are compatible with UNIBUS PDP-11 systems. Each formatter will support only one magnetic tape transport. Up to four TS11 subsystems are supported on PDP-11 and VAX-11/780 systems. Up to two TS11 subsystems are supported on VAX-11/750 systems.

## **RECORDING METHODS**

The TS11 writes data in PE (Phase-Encoded) mode at 1600 b/in. Data is written on the tape by magnetizing small sections of the oxide on the tape in different directions, i.e. either positively or negatively. A change or lack of change in the direction between adjacent magnetized sections of tape, depending on the recording method used, indicates whether the bit they represent is a 1 or a 0. In PE mode, a change in direction from positive to negative represents a 1 bit and a change in direction from negative to positive represents a 0 bit.

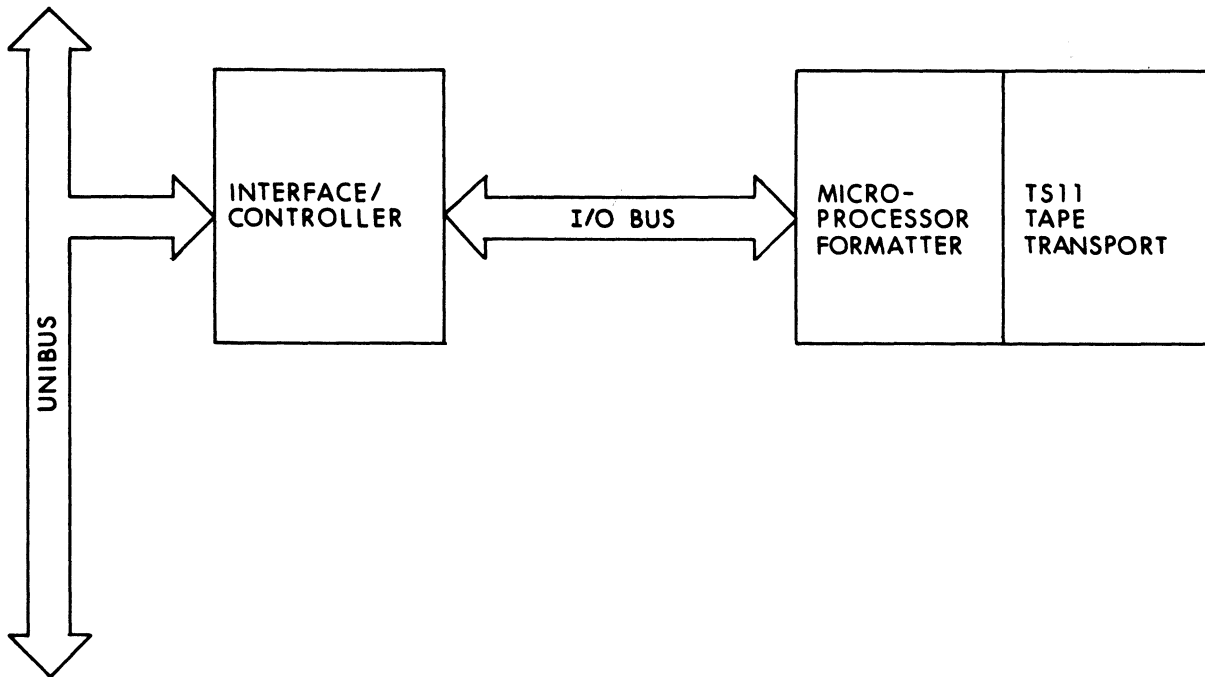


Figure 3-4 TS11 SYSTEM BLOCK DIAGRAM

At the beginning of a tape to be written in PE mode, the tape formatter writes a 6 inch identification burst between the BOT marker and the first data record. When writing a record, the tape formatter writes a preamble, the data bytes of the record one by one, a postamble, and then slows the tape down to a stop. The preamble and the postamble are used for synchronizing the data clock circuitry in the tape formatter.

### **DATA ORGANIZATION**

The head assembly of a nine-track magnetic tape transport, such as the TS11, consists of one erase head, nine write heads, and nine read heads. The nine read and the nine write heads correspond to the lengthwise tracks of the tape, i.e one read head and one write head for each track. The write head is an electromagnet used to magnetize small sections on the tape. The read head senses flux changes (changes in magnetic direction) on the tape and the erase head erases all information by magnetizing the whole width of the tape all in the same direction.

In order to write the 16-bit data from the processor onto the nine tracks of the TS11, the tape formatter divides each 16-bit memory word into two 8-bit bytes and generates a parity bit for each byte. The formatter then transfers these 8-bit bytes plus the parity bits to the tape head assembly. Each bit corresponds to one read and one write head, i.e. one track on the tape. Thus, one 8-bit byte of data plus parity is written across the width of the magnetic tape. These data bytes or tape characters each with its parity bit are written one at a time in groups called records or blocks. The length of a record is software controlled, but is typically between 12 and 2,000 bytes. The maximum block size allowed by the hardware is 65 KB. The tape formatter always stops the tape motion between records leaving a 0.6 inch inter-record (IRG) or interblock (IBG) gap of blank tape. This gap must be at least 0.6 inches and can become as long as 25 ft by repeatedly erasing a bad block and retrying the WRITE operation further down the tape.

A tape mark is a special short record used by programmers as a software flag. When executing a READ command the tape formatter will find either data to be read or a tape mark on the tape. When the formatter finds a tape mark it stops reading the tape and reports the tape mark to the processor by setting the TAPE MARK bit in the drive status register. Usually one tape mark indicates the end of a file while two tape marks in a row indicate the logical end of the tape.

## OPERATION

The TS11 formatter has two registers: the Status Register and the Bus Address/Data Buffer Register. The Bus Address Register (TSBA) is loaded with the control program address. If this register is read it may contain a UNIBUS address, status information, or data, depending on the operation the TS11 is currently executing. The register is then referred to as the Data Buffer Register (TSDB). The TS11 also references five extended status words, which function like registers, and are stored in memory locations. (Refer to the register section at the back of this book for register and extended status word diagrams and bit definitions.)

Before a READ operation can begin, the processor assembles a four-word control program which specifies that a READ operation is to be performed, the starting memory address where the data read off the tape is to be stored, and the number of bytes to be read off the tape (byte count). The processor then loads the address of the control program into the bus address register. The TS11 microprocessor-controlled formatter reads the control program from memory and executes the READ operation. An 8-bit byte of data is read off of the tape and then transferred to the formatter which checks the parity. Two 8-bit bytes (one 16-bit word) are stored in the formatter which generates a parity bit for each 16-bit word which is then written into the memory location specified. This process continues until the proper byte count is reached or until the end of the record, whichever comes first. Only one record can be read at a time. The formatter then writes status information into the status register as well as seven additional status words into the memory location specified by the last SET CHARACTERISTICS command. Finally, the microprocessor-controlled formatter generates an interrupt to alert the processor that the data has been read off the tape.

Before a WRITE operation can begin, the processor assembles a four-word control program which specifies that a WRITE operation is to be performed, the starting memory address where the data to be written onto the tape is stored, and the number of bytes to be written onto the tape. The processor then loads the address of the control program into the bus address register. The TS11 microprocessor-controlled formatter reads the control program from memory and executes the WRITE operation. A 16-bit word of data is read from memory and then transferred to the formatter which checks the parity. The formatter then splits the 16-bit word into two 8-bit bytes and generates a parity bit for each 8-bit byte and then writes the bytes on the tape one by one.



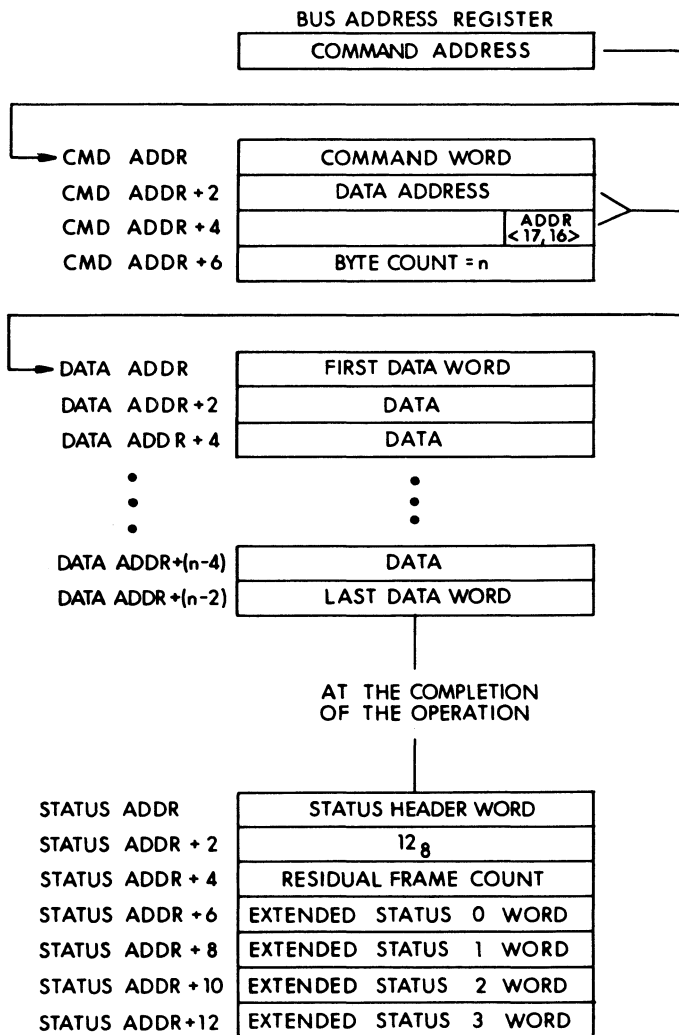


Figure 3-5 READ/WRITE operation sequence

This process continues until the proper byte count is reached. The formatter then writes status information into the status register as well as seven additional status words into the memory location specified by the last SET CHARACTERISTICS command. Finally, the microprocessor-controlled formatter generates an interrupt to alert the processor that the data has been written onto the tape.

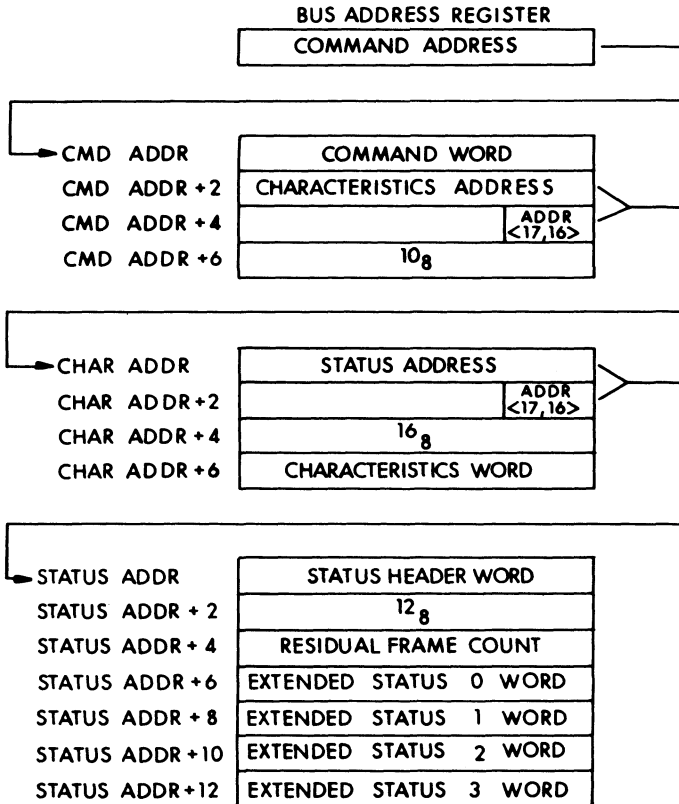


Figure 3-6 SET CHARACTERISTICS operation sequence

Other operations include: READ BACKWARD, WRITE TAPE MARK, ERASE GAP, SPACE FORWARD, SPACE BACKWARD, REWIND, REWIND/UNLOAD.

### **DATA INTEGRITY**

Several error checking and correction features of the TS11 ensure that the data has correct parity.

The parity error checking circuitry checks characters one by one during a READ operation. Similarly, the read-after-write circuitry checks characters one by one during a WRITE operation to ensure that the data just written has correct parity. The self-clocking feature of PE recorded data allows on-the-fly single-track error correction by detecting and reconstructing lost data during a READ operation.

An industry-standard file-protect ring on the tape reel prevents accidental writing on that tape. The operator should remove the ring when the tape reel is stored and insert it only when mounting the tape reel before a WRITE operation.

### **INTERRUPTS**

The TS11 magnetic tape system formatter uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the last control program is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the SPECIAL CONDITION bit or the READY bit in the status register is set.

When the SPECIAL CONDITION bit is set, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the formatter has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 224. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

**RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the magnetic tape system. Special design features of the TS11 magnetic tape systems give them these qualities of high reliability as well as ease of maintenance.

- Modular construction of the TS11 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Integral microprocessor-controlled diagnostics allow for self-testing when the TS11 is in Idle mode.
- Off-line microprocessor-controlled diagnostic capability allows the TS11 to be serviced independent of the host processor.
- On-line microprocessor-controlled diagnostic capability alerts the host processor to microprocessor failure.
- Customer Confidence Checks allow the user to verify subsystem operation.

LOAD REW UNLD	ON- LINE	MICRO OK	VOL VALID	DENS ERROR	WRITE LOCK	BOT	EOT
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Figure 3-7 TS11 FRONT PANEL CONTROLS AND INDICATORS

**PANEL CONTROLS AND INDICATORS**

The front panel controls allow the operator to control the tape transport manually and perform diagnostics when it is off-line. When on-line the transport is under program control except for taking it off-line. The indicator lights provide transport status information.

- **LOAD/REW/UNLD** (LOD in some versions) switch (momentary pushbutton/green light indicator on front panel)

Depressing this switch after the tape has been threaded causes the transport to load the tape and the indicator to light. Depressing this switch when the tape has been loaded and is not at BOT causes the tape to rewind to BOT. Depressing this switch when the tape is at BOT causes the transport to unload the tape. Note that the rewind and unload functions are operational only when the tape transport is off-line.

- ON-LINE (ONL in some versions) switch (alternate-action pushbutton/blue light indicator on front panel)

Depressing this switch causes the tape transport to go on-line and the indicator to light. Depressing it again causes the tape transport to go off-line and the indicator light to go out.

- MICRO OK (UOK in some versions) lamp (white light indicator on front panel)

When lit, this lamp indicates that the microprocessor-controlled formatter is operating with no errors.

- VOL VALID (VCK in some versions) lamp (white light indicator on front panel)

When lit, this lamp indicates a change in the tape transport status, i.e. that the transport has gone on-line or off-line since the last processor command.

- DENS ERROR (DCK in some versions) lamp (white light indicator on front panel)

When lit, this lamp indicates that an invalid identification burst (IDB), indicating that the tape was not written in PE, was sensed at BOT. However, the tape can still be read if IDB is incorrect and the tape is actually written in PE.

- WRITE LOCK (WLK in some versions) lamp (white light indicator on front panel)

When lit, this lamp indicates that either no tape reel has been mounted or that a reel without a file-protect ring has been mounted onto a transport.

- BOT (Beginning Of Tape) lamp (white light indicator on front panel)

When lit, this lamp indicates that the tape is at BOT.

- EOT (End Of Tape) lamp (red light indicator on front panel)

When lit, this lamp indicates that the tape has passed the EOT marker. Note that manually moving the tape past EOT will not cause the indicator to light.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Freestanding
Controller mounting code	One hex slot

## MAGNETIC TAPES

### Height

TS11-BA(BB)	60 in (152.4 cm)
TS11-CA(CB)	60.5 in (153.7 cm)
TS11-DA(DB)	72 in (182.9 cm)

### Width

TS11-BA(BB)	28 in (71 cm)
TS11-CA(CB)	21.5 in (54.6 cm)
TS11-DA(DB)	21.25 in (54.1 cm)

### Depth

TS11-BA(BB)	30 in (76.2 cm)
TS11-CA(CB)	30 in (76.2 cm)
TS11-DA(DB)	30 in (76.2 cm)

### Weight

TS11-BA(BB)	555 lbs (252 kg)
TS11-CA(CB)	382 lbs (173.4 kg)
TS11-DA(DB)	348 lbs (158 kg)

## PERFORMANCE

Transports per formatter	1
Recording density	1600 b/in
Read/write speed	45 in/s
Capacity per 2400 ft reel	40 MB with 8 KB blocks
Rewind speed	150 in/s
Rewind time	2 min per 2400 ft reel
Peak transfer speed	72 KB/s
Maximum load/unload time	8s

## ELECTRICAL

Operating current	10 A at 120 Vac 5 A at 240 Vac
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## MAGNETIC TAPES

Interface (controller) current	3.5 A maximum at +5 Vdc 1.5 A typical at +5 Vdc
Power consumption	1200 Watts maximum
Heat dissipation	4092 Btus/hr maximum
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%

Phase	1-Phase
Line frequency	60 Hz $\pm$ 3 Hz 50 Hz $\pm$ 3 Hz

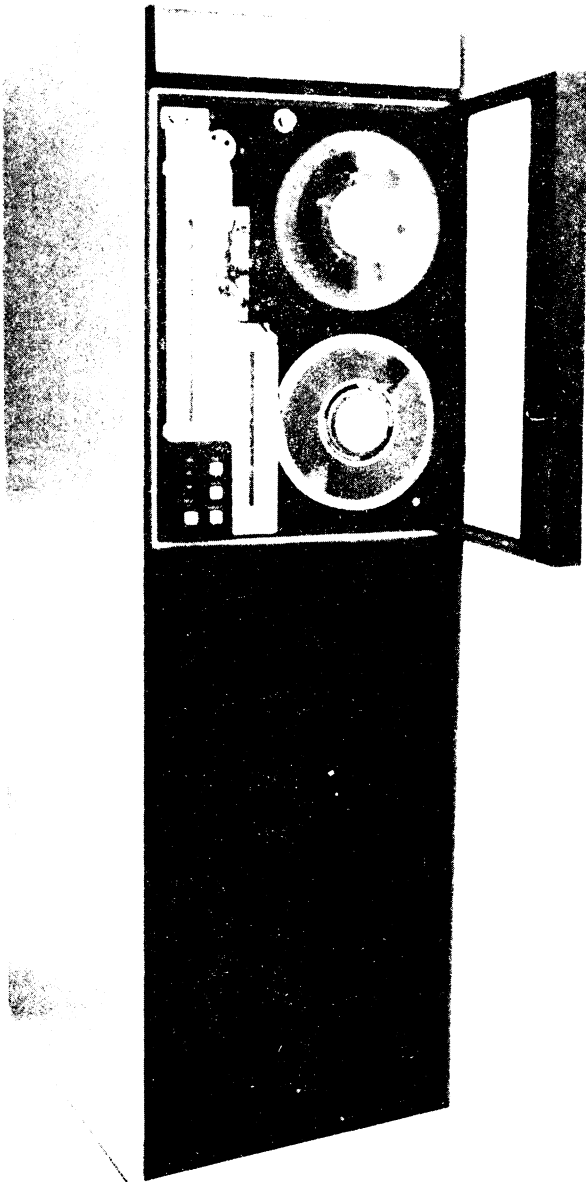
### Receptacles

TS11-BA(BB), TS11-DA(DB)	NEMA #L5-30R (120 Vac), NEMA #L6-20R (240 Vac)
TS11-CA(CB)	NEMA #L5-30R (120 Vac), NEMA #L6-15R (240 Vac)

Line cord length	12 ft
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### ENVIRONMENTAL

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	77°F (25°C)
Maximum operating altitude	8,000 ft (2438 m) above sea level



TE 16



## TE16

The TE16 is a 9-track, bolt-on, tape storage system which connects to the MASSBUS via the controller/adaptor. The TJE16 subsystems are supported by UNIBUS PDP-11 systems except the PDP-11/70, the TWE16 subsystems are supported by PDP-11/70 systems only, and the TEE16 subsystems are supported by VAX-11/780 systems. The TE16 was designed to operate at medium speeds in moderate usage environments in a variety of applications, such as disk-to-tape backup for small to medium disks, software distribution medium, and tape interchange.

## FEATURES

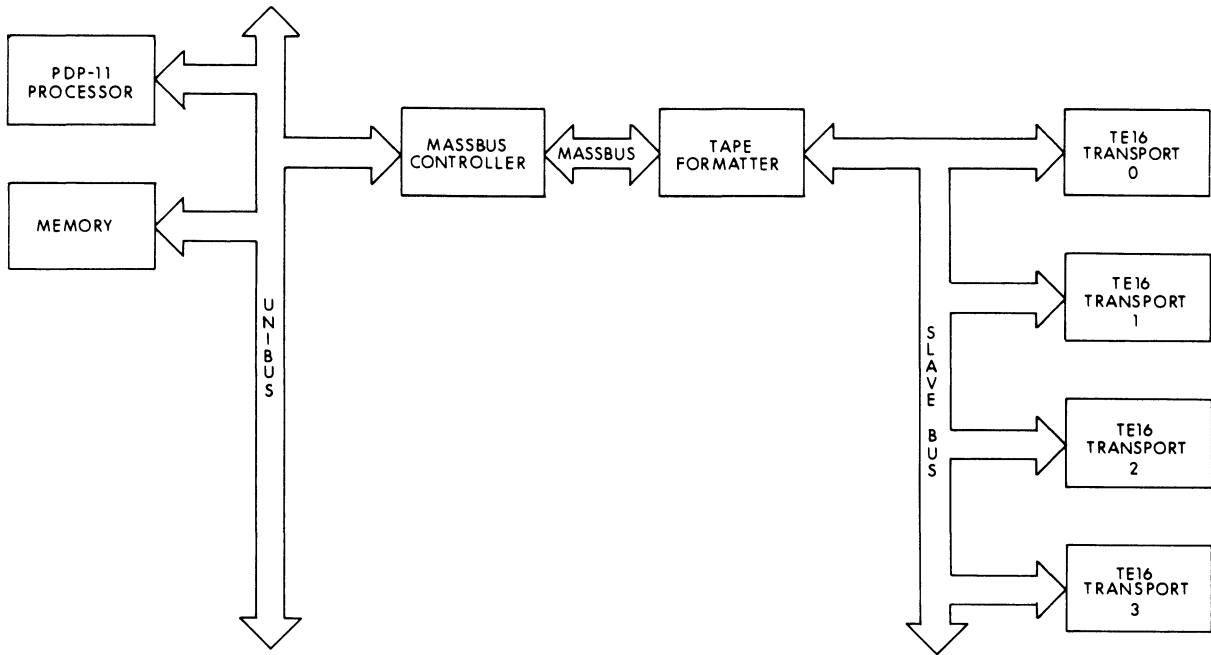
- Program-selectable recording at 1600 b/in (PE) or 800 b/in (NRZI)
- Read/write speeds of 45 in/s
- Automatic density select on a READ operation (1600 b/in or 800 b/in)
- Expandable up to a total of eight tape transports per subsystem
- Direct Memory Access (DMA) data transfers
- Vacuum column tape buffering

## DESCRIPTION

The TJE16, the TWE16, and the TEE16 magnetic tape storage subsystems consist of a freestanding tape transport (-AA, AD versions are in H9602 cabinets and -EA, ED versions are in H960 cabinets), a tape formatter and its power supply mounted in the transport cabinet, a MASSBUS controller/adaptor, and a MASSBUS cable. Up to seven more add-on TE16-AE(AJ) or TE16-EE(EJ) transports may be added to any of the three subsystems.

## RECORDING METHODS

The TE16 writes data in two modes: NRZI (Non-Return to Zero Inverted) at 800 b/in and PE (Phase-Encoded) at 1600 b/in. Data is written on the tape by magnetizing small sections of the oxide on the tape in different directions, ie. either positively or negatively. A change or lack of change in the direction between adjacent magnetized sections of tape, depending on the recording method used, indicates whether the bit represented is a 1 bit or a 0 bit. In NRZI mode, a change in direction from negative to positive or from positive to negative represents a 1 bit and a lack of change in direction represents a 0 bit. In PE mode, a change in direction from positive to negative represents a 1 bit and a change in direction from negative to positive represents a 0 bit.



MAGNETIC TAPES

UP TO 4 MORE TE16  
TRANSPORTS FOR A  
TOTAL OF 8

Figure 3-8 TJE16 SYSTEM BLOCK DIAGRAM

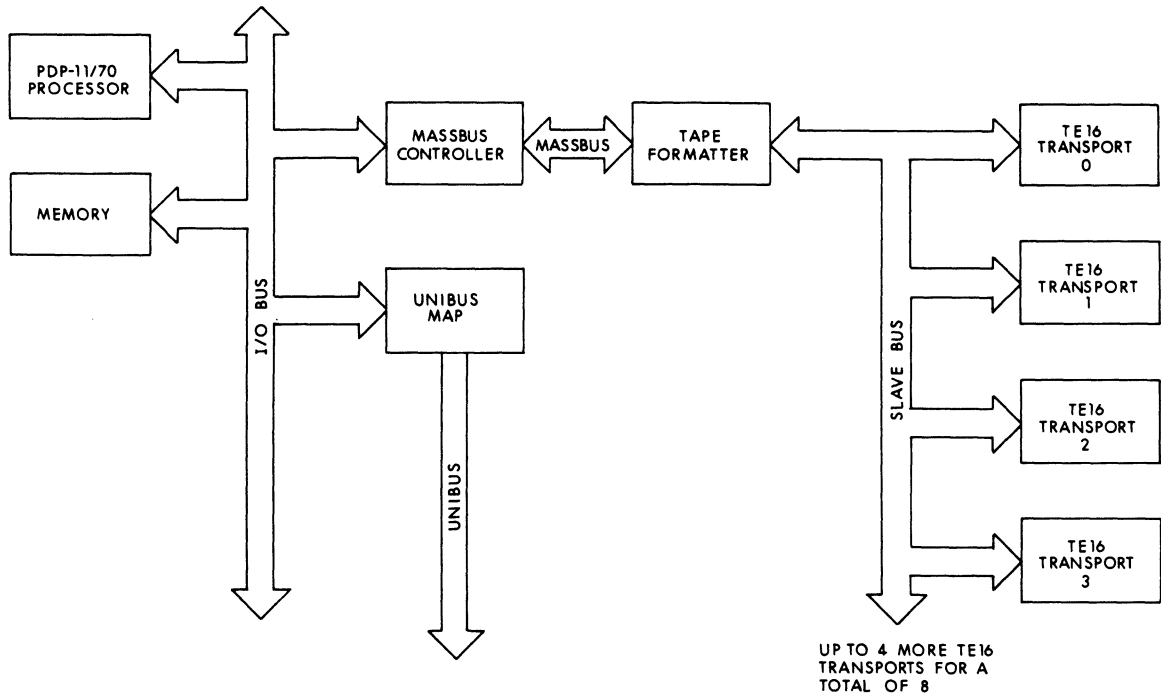
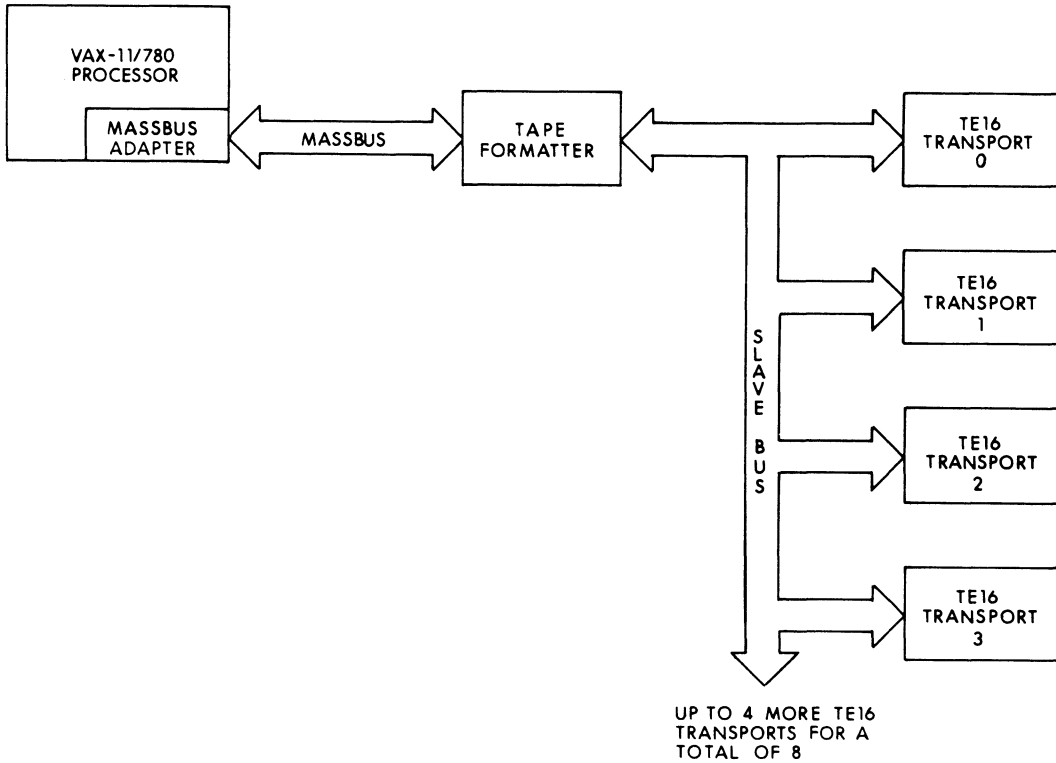


Figure 3-9 TWE16 SYSTEM BLOCK DIAGRAM



MAGNETIC TAPES

Figure 3-10 TEE16 SYSTEM BLOCK DIAGRAM

At the beginning of a tape to be written in NRZI mode, the tape formatter leaves an initial gap of 3.2 inches between the BOT marker and the first data record. When writing a record in NRZI mode, the tape transport writes the data bytes of the record one by one, a CRC character (Cyclic Redundancy Check) and an LRC character (Longitudinal Redundancy Check), and then slows the tape down to a stop.

At the beginning of a tape to be written in PE mode, the tape formatter writes a 6 inch identification burst between the BOT marker and the first data record. When writing a record in PE mode, the tape formatter writes a preamble, the data bytes of the record one by one, a postamble, and then slows the tape down to a stop. The preamble and the postamble are used for synchronizing the data clock circuitry in the tape formatter.

### **DATA ORGANIZATION**

The head assembly of a nine-track magnetic tape transport, such as the TE16, consists of one erase head, nine write heads, and nine read heads. The nine read and the nine write heads correspond to the lengthwise tracks of the tape, i.e one read head and one write head for each track. The write head is an electromagnet used to magnetize small sections on the tape. The read head senses flux changes (changes in magnetic direction) on the tape and the erase head erases all information by magnetizing the whole width of the tape all in the same direction.

In order to write the 16-bit data from the processor onto the nine tracks of the TE16, the tape formatter divides each 16-bit memory word into two 8-bit bytes and generates a parity bit for each byte. The formatter then transfers these 8-bit bytes plus the parity bits to the tape head assembly. Each bit corresponds to one read and one write head, i.e. one track on the tape. Thus, one 8-bit byte of data plus parity is written across the width of the magnetic tape. These data bytes or tape characters each with its parity bit are written one at a time in groups called records or blocks. The length of a record is software controlled, but is typically between 12 and 2,000 bytes. The maximum block size allowed by the hardware is 65 KB. A record containing twelve characters or less will cause the NON-STANDARD GAP bit in the error register to be set. This short record detect feature can be bypassed by a jumper in the tape formatter. The tape formatter always stops the tape motion between records leaving a 0.6 inch interrecord (IRG) or interblock (IBG) gap of blank tape. This gap must be at least 0.6 inches and can become as long as 25 ft by repeatedly erasing a bad block and retrying the WRITE operation further down the tape.

A tape mark is a special short record used by programmers as a software flag. When executing a READ command the tape formatter will find either data to be read or a tape mark on the tape. When the formatter finds a tape mark it stops reading the tape and reports the tape mark to the processor by setting the TAPE MARK bit in the drive status register. Usually one tape mark indicates the end of a file while two tape marks in a row indicate the logical end of the tape.

## **OPERATION**

The TJE16 subsystems have 20 registers, the TWE16 subsystems have 22 registers, and the TEE16 subsystems have 16 registers plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ operation can begin the processor loads the bus address, word count, tape control, and control and status 1 registers respectively.

The bus address register specifies the starting memory address of the desired storage location for the data to be read off the tape. The word count register specifies the number of words to be read off the tape and stored in memory while the tape control register selects which of the available transports (up to 8 per formatter) is to perform the READ operation.

After the bus address, word count, and tape control registers have been loaded, the control and status 1 register is loaded with the READ command from the processor. The READ command is then executed. An 8-bit byte of data is read off of the tape and then transferred to the formatter which checks the parity. Two 8-bit bytes (one 16-bit word) are stored in the formatter which generates a parity bit for each 16-bit word which is then written into the memory location specified. This process continues until the proper word count is reached or until the end of the record, whichever comes first. Only one record can be read at a time. When the tape stops, an interrupt is set to alert the processor that the data has been read off the tape.

Before a WRITE operation can begin the processor loads the bus address, word count, frame count, tape control, and control and status 1 registers respectively.

The bus address register specifies the starting memory address of the data to be written onto the tape. The word count register specifies the number of words to be written onto the tape while the tape control register selects which of the available transports is to perform the WRITE operation. The tape control register also specifies the desired

recording mode: NRZI or PE. The frame count register specifies the number of bytes to be written on the tape (twice the word count).

After the bus address, word count, frame count, and tape control registers have been loaded, the control and status 1 register is loaded with the WRITE command from the processor. The WRITE command is then executed. A 16-bit word of data is read from memory and then transferred to the formatter which checks the parity. The formatter divides the 16-bit word into two 8-bit bytes and generates a parity bit for each 8-bit byte and writes the bytes on the tape one by one. This process continues until the proper frame count is reached. When the tape stops, an interrupt is set to alert the processor that the data has been written onto the tape.

Other operations include: READ BACKWARD, WRITE TAPE MARK, ERASE GAP, SPACE FORWARD, SPACE BACKWARD, REWIND, REWIND/UNLOAD.

The automatic density select feature on a READ operation (1600 b/in or 800 b/in) can be disabled by a jumper in the tape formatter.

### **DATA INTEGRITY**

Several error checking and correction features of the TE16 ensure that the data has correct parity.

In NRZI mode, the parity error checking circuitry checks characters one by one during a READ operation and the read-after-write circuitry checks characters one by one during a WRITE operation. NRZI mode also includes a cyclic redundancy check (CRC) character and a longitudinal redundancy check (LRC) character. During a WRITE operation the CRC character is generated and written on the tape at the end of each record. During a READ operation the data read is used to generate a second CRC character which is then compared to the CRC read from the end of the record. If there is a discrepancy between the two CRC characters, a bit is set in the error register. During a WRITE operation the LRC character is generated and written on the tape at the end of each record, after the CRC. The LRC character consists of nine parity bits (one for each track). During a READ operation the data read is used to generate a second LRC character which is then compared to the LRC read from the end of the record. If there is a discrepancy between the two LRC characters, a bit is set in the error register.

The formatter hardware can correct a single bad bit in a NRZI block during a software retry. If a READ FORWARD operation fails due to a data parity error and the software then commands a READ BACKWARD or SPACE BACKWARD followed by a retry of the READ FORWARD operation, the error correction circuitry is automatically

invoked. At the end of the record the CRC and LRC checks are used to verify that the correction was successful.

In PE mode, the parity error checking circuitry checks characters one by one during a READ operation. Similarly, the read-after-write circuitry checks characters one by one during a WRITE operation to ensure that the data just written has correct parity. The self-clocking feature allows on-the-fly single-track error correction by detecting and reconstructing lost data during a READ operation.

An industry-standard file-protect ring on the tape reel prevents accidental writing on that tape. The operator should remove the ring when the tape reel is stored and insert it only when mounting the tape reel before a WRITE operation.

### **INTERRUPTS**

The TE16 magnetic tape system controller uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status 1 register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the SPECIAL CONDITION or READY bit in the control and status 1 register is also set.

When the SPECIAL CONDITION bit is set, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the controller has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 224. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the magnetic tape system. Special design features of the TE16 magnetic tape systems give them these qualities of high reliability as well as ease of maintenance.

- Modular construction of the TE16 enables parts to be quickly removed and replaced during routine servicing and maintenance.



## MAGNETIC TAPES

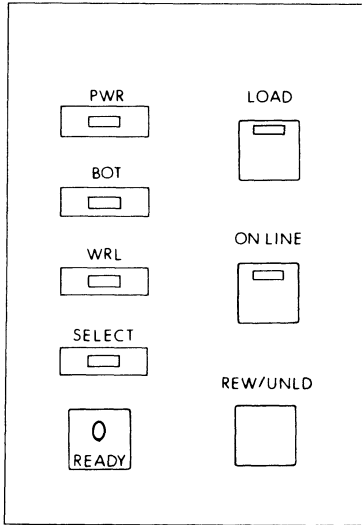


Figure 3-11 TE16 FRONT PANEL CONTROLS AND INDICATORS

### PANEL CONTROLS AND INDICATORS

The front panel controls allow the operator to control the tape transport manually when it is off-line. When on-line the transport is under program control except for taking it off-line. The indicator lights provide transport status information.

- PWR (POWER) lamp (yellow light indicator on front panel)  
When lit, this lamp indicates that the transport is turned on.
- BOT (Beginning Of Tape) lamp (yellow light indicator on front panel)  
When lit, this lamp indicates that the tape is at BOT.
- WRL (WRITE LOCK) lamp (red light indicator on front panel)  
When lit, this lamp indicates that a reel without a file-protect ring has been mounted onto a transport.
- SELECT lamp (yellow light indicator on front panel)  
This indicator lights on the on-line transport (0-7) selected by the processor.
- TRANSPORT SELECT receptacle (unlabeled receptacle on front panel)  
Each transport comes with eight numbered (0-7) plugs. The transport number is set by inserting one of the numbered plugs into the receptacle. If no plug is in the receptacle, that transport cannot be selected by the processor. Note that drive number units cannot be duplicated.

## MAGNETIC TAPES

- **LOAD** switch (momentary pushbutton/yellow light indicator on front panel)

Depressing this switch after the tape has been threaded causes the transport to load the tape and the indicator to light.

- **ON-LINE** switch (alternate-action pushbutton/yellow light indicator on front panel)

Depressing this switch causes the tape transport to go on-line and the indicator to light. Depressing it again causes the tape transport to go off-line and the indicator light to go out.

- **REW/UNLD (REWIND/UNLOAD)** switch (momentary pushbutton on front panel)

Depressing this switch causes the tape to rewind to BOT. Depressing this switch when the tape is at BOT causes the transport to unload the tape.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Bolt-on
Controller mounting code	
TJE16	2 SUs
TWE16	MASSBUS port
TEE16	Option panel space
Height	
TE16-AE(AJ)	60 in (152.4 cm)
TE16-EE(EJ)	72 in (182.9 cm)
Width	
TE16-AE(AJ)	28 in (71 cm)
TE16-EE(EJ)	21 in (53.3 cm)
Depth	
TE16-AE(AJ)	30 in (76.2 cm)
TE16-EE(EJ)	31 in (78.7 cm)
Weight	
TE16-AE(AJ)	500 lbs (254 kg)
TE16-EE(EJ)	500 lbs (254 kg)

## MAGNETIC TAPES

### PERFORMANCE

Transports per controller	8
Recording density	1600/800 b/in
Read/write speed	45 in/s
Capacity per 2400 ft reel	
1600 b/in	40 MB with 8 KB blocks
800 b/in	20 MB with 8 KB blocks
Rewind speed	150 in/s
Rewind time	3.7 min per 2400 ft reel
Peak transfer speed	
1600 b/in	72 KB/s
800 b/in	36 KB/s

### ELECTRICAL

Starting (surge) current	85 A at 120 Vac 42.5 A at 240 Vac
Surge duration	100 ms
Operating current	9 A at 120 Vac (subsystem) 4.5 A at 240 Vac (subsystem) 6.5 A at 120 Vac (add-on drive) 3.25 A at 240 Vac (add-on drive)
Power consumption	1200 Watts maximum (subsystem) 900 Watts maximum (add-on drive)
Heat dissipation	4100 Btus/hr maximum (subsystem) 3100 Btus/hr maximum (add-on drive)
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	60 Hz $\pm$ 3 Hz 50 Hz $\pm$ 3 Hz

## MAGNETIC TAPES

Receptacle	NEMA #L5-30R (120 Vac), NEMA #L6-20R (240 Vac)
Line cord length	10 ft
<b>ENVIRONMENTAL</b>	
Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	77°F (25°C)
Maximum operating altitude	8,000 ft (2440 m) above sea level

*MAGNETIC TAPES*



**TU77**

**TU77**

The TU77 is a nine-track, freestanding, magnetic tape storage system which connects to the processor via the MASSBUS controller/adaptor. The TJU77 subsystems are supported by UNIBUS PDP-11 systems except the PDP-11/70, the TWU77 subsystems are supported by PDP-11/70 systems only, the TEU77 subsystems are supported by VAX-11/780 systems, and the TGU77 subsystems are supported by VAX-11/750 systems. The TU77 was designed to operate at high speeds in high usage environments in a wide range of applications, such as fast disk-to-tape backup, data acquisition, heavy transaction processing/journaling, and tape interchange.

**FEATURES**

- Program-selectable recording at 1600 b/in (PE) or 800 b/in (NRZI)
- Read/write speed of 125 in/s
- Automatic tape threading of 10.5 in tape reels as well as IBM Easy Load #1 and #2™ type tape cartridges
- Automatic density select on a READ operation (1600 b/in or 800 b/in)
- Expandable up to a total of four tape transports per subsystem
- Direct Memory Access (DMA) data transfers
- Vacuum column tape buffering

**DESCRIPTION**

The TJU77, the TWU77, the TEU77, and the TGU77 magnetic tape storage subsystems consist of a freestanding tape transport in an H9602 cabinet, a tape formatter and its power supply mounted in the transport cabinet, a MASSBUS controller/adaptor, and a MASSBUS cable. Up to three more add-on TU77-AF(AJ) transports may be added to any of the four subsystems.

**RECORDING METHODS**

The TU77 writes data in two modes: NRZI (Non-Return to Zero Inverted) at 800 b/in and PE (Phase-Encoded) at 1600 b/in. Data is written on the tape by magnetizing small sections of the oxide on the tape in different directions, i.e. either positively or negatively. A change or lack of change in the direction between adjacent magnetized sections of tape, depending on the recording method used, indicates whether the bit represented is a 1 or a 0. In NRZI mode, a change in direction from negative to positive or from positive to negative represents a 1 bit and a lack of change in direction represents a 0 bit. In PE mode, a change in direction from positive to negative represents a 1 bit and a change in direction from negative to positive represents a 0 bit.

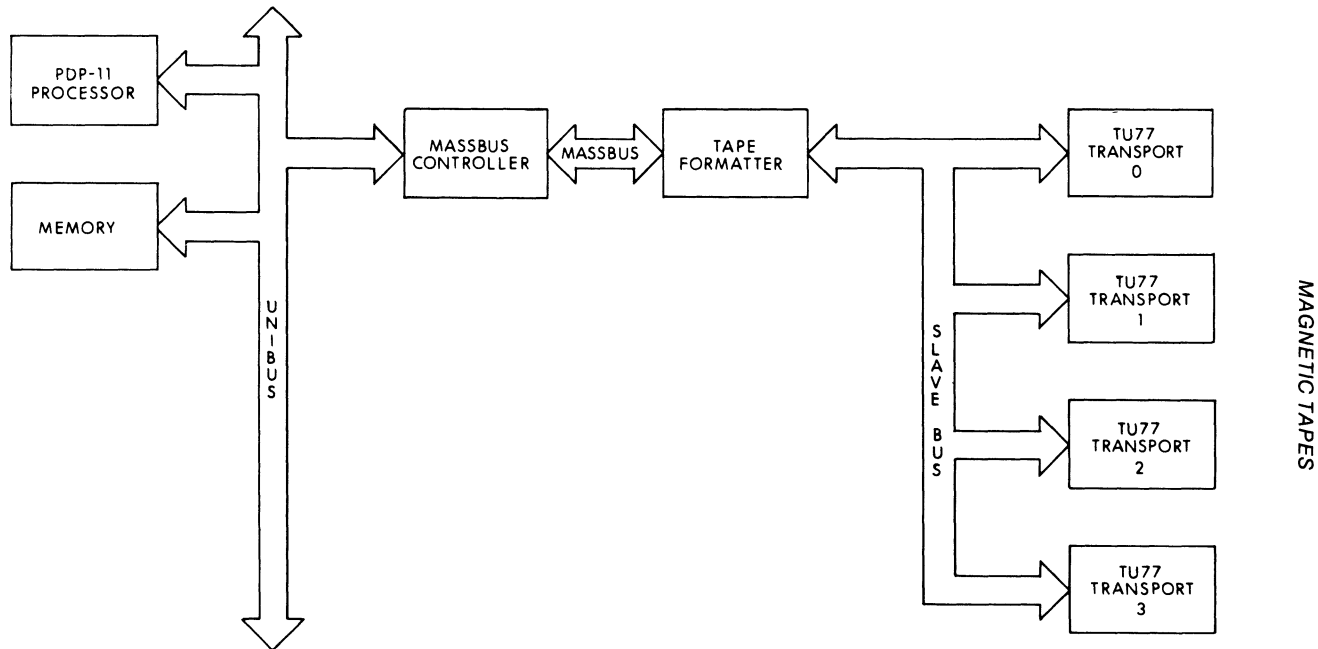


Figure 3-12 TJU77 SYSTEM BLOCK DIAGRAM



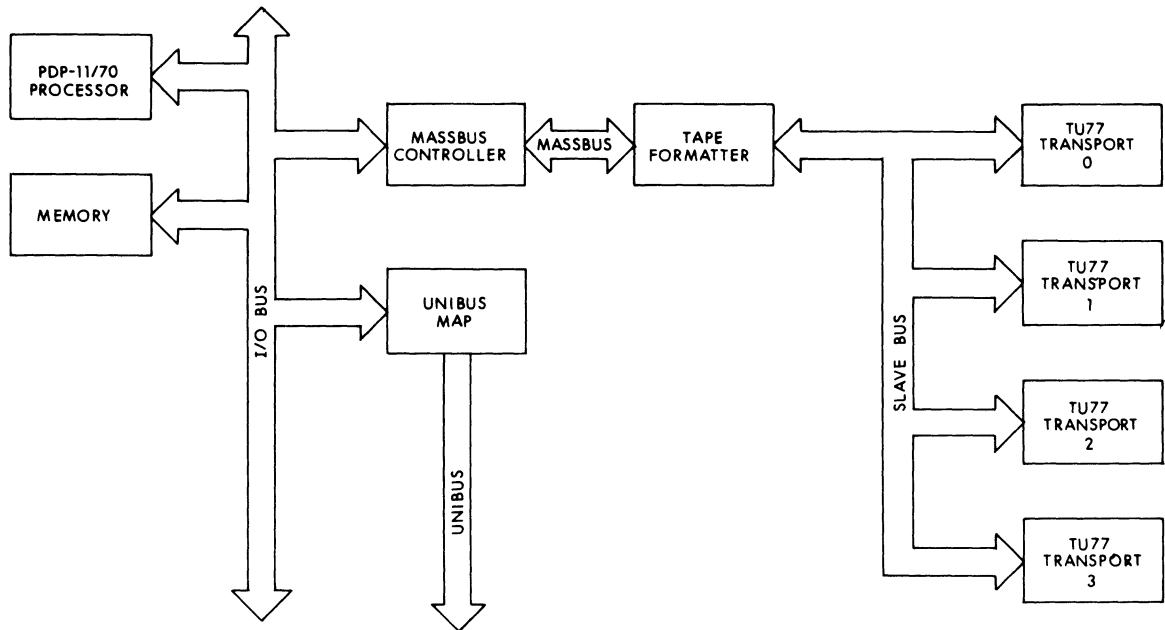


Figure 3-13 TWU77 SYSTEM BLOCK DIAGRAM

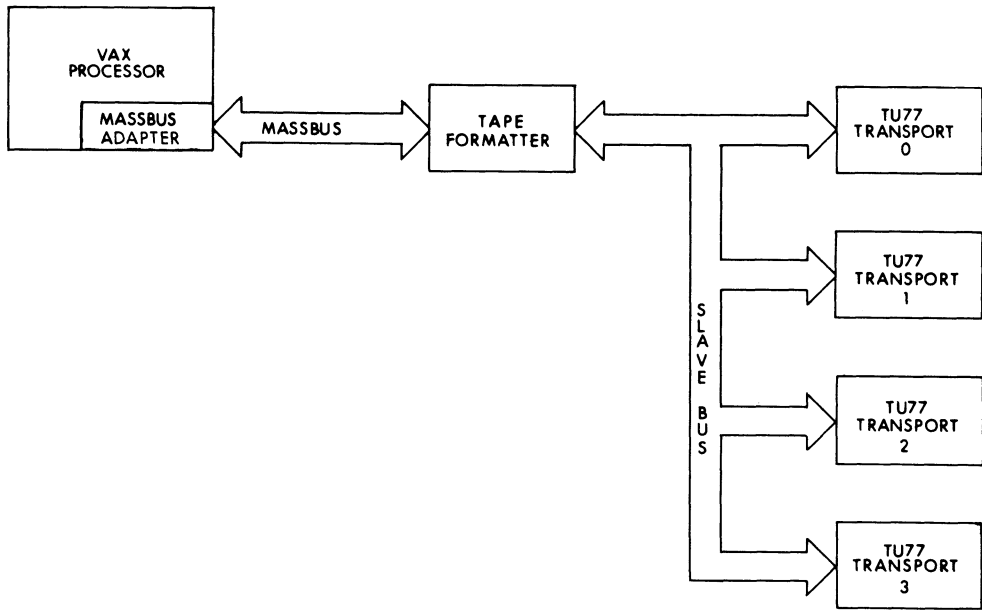


Figure 3-14 TEU77/TGU77 SYSTEM BLOCK DIAGRAM

At the beginning of a tape to be written in NRZI mode, the tape formatter leaves an initial gap of 3.2 inches between the BOT marker and the first data record. When writing a record in NRZI mode, the tape transport writes the data bytes of the record one by one, a CRC character (Cyclic Redundancy Check) and an LRC character (Longitudinal Redundancy Check), and then slows the tape down to a stop.

At the beginning of a tape to be written in PE mode, the tape formatter writes a 6 inch identification burst between the BOT marker and the first data record. When writing a record in PE mode, the tape formatter writes a preamble, the data bytes of the record one by one, a postamble, and then slows the tape down to a stop. The preamble and the postamble are used for synchronizing the data clock circuitry in the tape formatter.

### **DATA ORGANIZATION**

The head assembly of a nine-track magnetic tape transport, such as the TU77, consists of one erase head, nine write heads, and nine read heads. The nine read and the nine write heads correspond to the lengthwise tracks of the tape, i.e one read head and one write head for each track. The write head is an electromagnet used to magnetize small sections on the tape. The read head senses flux changes (changes in magnetic direction) on the tape and the erase head erases all information by magnetizing the whole width of the tape all in the same direction.

In order to write the 16-bit data from the processor onto the nine tracks of the TU77, the tape formatter divides each 16-bit memory word into two 8-bit bytes and generates a parity bit for each byte. The formatter then transfers these 8-bit bytes plus the parity bits to the tape head assembly. Each bit corresponds to one read and one write head, i.e. one track on the tape. Thus, one 8-bit byte of data plus parity is written across the width of the magnetic tape. These data bytes or tape characters, each with its parity bit, are written one at a time in groups called records or blocks. The length of a record is software controlled, but is typically between 12 and 2,000 bytes. The maximum block size allowed by the hardware is 65 KB. A record containing twelve characters or less will cause the NON-STANDARD GAP bit in the error register to be set. This short record detect feature can be bypassed by a jumper in the tape formatter. The tape formatter always stops the tape motion between records leaving a 0.6 inch interrecord (IRG) or interblock (IBG) gap of blank tape. This gap must be at least 0.6 inch and can become as long as 25 ft by repeatedly erasing a bad block and retrying the WRITE operation further down the tape.

A tape mark is a special short record used by programmers as a software flag. When executing a READ command, the tape formatter will find either data to be read or a tape mark on the tape. When the formatter finds a tape mark, it stops reading the tape and reports the tape mark to the processor by setting the TAPE MARK bit in the drive status register. Usually, one tape mark indicates the end of a file, while two tape marks in a row indicate the logical end of the tape.

## **OPERATION**

The TJU77 subsystems have 20 registers, the TWU77 subsystems have 22, and the TEU77 and the TGU77 subsystems have 16 plus the MASSBUS adapter registers. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Before a READ operation can begin, the processor loads the bus address, word count, tape control, and control and status 1 registers, respectively.

The bus address register specifies the starting memory address of the storage location for the data to be read off the tape. The word count register specifies the number of words to be read off the tape and stored in memory while the tape control register selects which of the available transports (up to 4 per formatter) is to perform the READ operation.

After the bus address, word count, and tape control registers have been loaded, the control and status 1 register is loaded with the READ command from the processor. The READ command is then executed. An 8-bit byte of data is read off the tape and then transferred to the formatter which checks the parity. Two 8-bit bytes (one 16-bit word) of data are stored in the formatter, which generates a parity bit for each 16-bit word. The 16-bit word plus parity is then written into the memory location specified. This process continues until the proper word count is reached or until the end of the record, whichever comes first. Only one record can be read at a time. When the tape stops, an interrupt is set to alert the processor that the data has been read off the tape.

Before a WRITE operation can begin, the processor loads the bus address, word count, frame count, tape control, and control and status 1 registers, respectively.

The bus address register specifies the starting memory address of the data to be written onto the tape. The word count register specifies the number of words to be written onto the tape while the tape control register selects which of the available transports is to perform the

WRITE operation. The tape control register also specifies the desired recording mode: NRZI or PE. The frame count register specifies the number of bytes to be written on the tape (twice the word count).

After the bus address, word count, frame count, and tape control registers have been loaded, the control and status 1 register is loaded with the WRITE command from the processor. The WRITE command is then executed. A 16-bit word of data is read from memory and then transferred to the formatter which checks the parity. The formatter divides the 16-bit word into two 8-bit bytes and generates a parity bit for each 8-bit byte and writes the bytes on the tape one by one. This process continues until the proper frame count is reached. When the tape stops, an interrupt is set to alert the processor that the data has been written onto the tape.

Other operations include: READ BACKWARD, WRITE TAPE MARK, ERASE GAP, SPACE FORWARD, SPACE BACKWARD, REWIND, REWIND/UNLOAD.

The automatic density select feature on a READ operation (1600 b/in or 800 b/in) can be disabled by a jumper in the tape formatter.

### **DATA INTEGRITY**

Several error checking and correction features of the TU77 ensure that the data has correct parity.

In NRZI mode, the parity error checking circuitry checks characters one by one during a READ operation and the read-after-write circuitry checks characters one by one during a WRITE operation. NRZI mode also includes a cyclic redundancy check (CRC) character and a longitudinal redundancy check (LRC) character. During a WRITE operation, the CRC character is generated and written on the tape at the end of each record. During a READ operation, the data read is used to generate a second CRC character which is then compared to the CRC read from the end of the record. If there is a discrepancy between the two CRC characters, a bit is set in the error register. During a WRITE operation the LRC character is generated and written onto the tape at the end of each record, after the CRC. The LRC character consists of nine parity bits (one for each track). During a READ operation, the data read is used to generate a second LRC character which is then compared to the LRC read from the end of the record. If there is a discrepancy between the two LRC characters, a bit is set in the error register.

The formatter hardware can correct a single bad bit in a NRZI block during a software retry. If a READ FORWARD operation fails due to a data parity error and the software then commands a READ BACKWARD or SPACE BACKWARD followed by a retry of the READ

FORWARD operation, the error correction circuitry is automatically invoked. At the end of the record, the CRC and the LRC are used to verify that the correction was successful.

In PE mode, the parity error checking circuitry checks characters one by one during a READ operation. Similarly, the read-after-write circuitry checks characters one by one during a WRITE operation to ensure that the data just written has correct parity. The self-clocking feature allows on-the-fly single-track error correction by detecting and reconstructing lost data during a READ operation.

An industry-standard file-protect ring on the tape reel prevents accidental writing on that tape. The operator should remove the ring when the tape reel is stored and insert it only when mounting the tape reel before a WRITE operation.

## **INTERRUPTS**

The TU77 magnetic tape system controller uses a vectored interrupt to cause the program to branch to an interrupt service routine. An interrupt can occur only if the INTERRUPT ENABLE bit in the control and status 1 register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the SPECIAL CONDITION or READY bit in the control and status 1 register is also set.

When the SPECIAL CONDITION bit is set, it indicates that some error or unusual condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the READY bit is set, the controller has successfully completed the operation and is ready to accept a command. An interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 5 and the interrupt vector address is 224. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy and uninterrupted processing of the magnetic tape system. Special design features of the TU77 magnetic tape systems give them these qualities of high reliability as well as ease of maintenance.

- Modular construction of the TU77 enables parts to be quickly removed and replaced during routine servicing and maintenance.

- Off-line test capability including motion and data flow allows the TU77 to be serviced independent of the host processor.

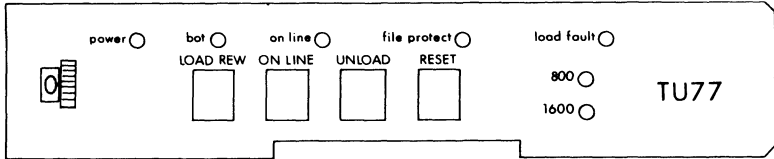


Figure 3-15 TU77 FRONT PANEL CONTROLS AND INDICATORS

### PANEL CONTROLS AND INDICATORS

The front panel controls allow the operator to control the tape transport manually when it is off-line. When on-line, the transport is under program control except for taking it off-line. The indicator lights provide transport status information.

- **TRANSPORT SELECT** switch (unlabeled thumbwheel on front panel)  
This switch sets the tape transport number (0-3).
- **LOAD/REWIND** switch (momentary pushbutton on front panel)  
Depressing this switch when the tape is not loaded causes the transport to load the tape. Depressing this switch when the tape is loaded causes the transport to rewind the tape to the beginning (BOT). This switch is operational only when the tape transport is off-line.
- **ON-LINE** switch (alternate-action pushbutton on front panel)  
Depressing this switch causes the tape transport to go on-line. Depressing it again causes the tape transport to go off-line.
- **UNLOAD** switch (momentary pushbutton on front panel)  
Depressing this switch causes the tape transport to rewind and then unload the tape. This switch is operational only when the tape transport is off-line.
- **RESET** switch (momentary pushbutton on front panel)  
Depressing this switch terminates all functions and causes the tape transport to go off-line. If the LOAD FAULT indicator is lit, depressing RESET causes it to go out.
- **POWER** lamp (red light indicator on front panel)  
When lit, this lamp indicates that the tape transport is turned on.

- **BOT (Beginning Of Tape) lamp (red light indicator on front panel)**  
When lit, this lamp indicates that the tape is at BOT.
- **ON-LINE lamp (red light indicator on front panel)**  
When lit, this lamp indicates that the tape transport is on-line. When not lit, this lamp indicates that the tape transport is off-line because  
1) the ON LINE switch has been depressed 2) the processor has issued a REWIND/UNLOAD command 3) a pneumatic failure has been detected or 4) the RESET switch has been depressed.
- **FILE PROTECT lamp (red light indicator on front panel)**  
When lit, this lamp indicates that a reel of tape without a file-protect ring has been loaded onto the tape transport.
- **LOAD FAULT lamp (red light indicator on front panel)**  
When lit, this lamp indicates that the automatic tape loading mechanism has failed to load the tape after two attempts.
- **800 lamp (red light indicator on front panel)**  
When lit, this lamp indicates that the tape transport is set to read or write at 800 b/in in NRZI mode.
- **1600 lamp (red light indicator on front panel)**  
When lit, this lamp indicates that the tape transport is set to read or write at 1600 b/in in PE mode.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Freestanding
Controller mounting code	
TJU77	2 SUs
TWU77	MASSBUS port
TEU77	Option panel space
TGU77	MBA slot
Height	60 in (152.4 cm)
Width	28 in (71 cm)
Depth	30 in (76.2 cm)
Weight	560 lbs (254 kg)



## MAGNETIC TAPES

### PERFORMANCE

Transports per formatter	4
Recording density	1600/800 b/in
Read/write speed	125 in/s
Capacity per 2400 ft reel	
1600 b/in	40 MB with 8 KB blocks
800 b/in	20 MB with 8 KB blocks
Rewind speed	440 in/s
Rewind time	70 s typical per 2400 ft reel
Load time	10 s without a retry
Peak transfer speed	
1600 b/in	200 KB/s
800 b/in	100 KB/s

### ELECTRICAL

Starting (surge) current	80 A at 240 Vac
Surge duration	1.2 s
Operating current	13 A at 240 Vac (subsystem) 11.5 at 240 Vac (add-on transport)
Power consumption	2295 Watts maximum (subsystem) 1914 Watts maximum (add-on transport)
Heat dissipation	7826 Btus/hr maximum (subsystem) 6527 Btus/hr maximum (add-on transport)
Operating voltage	220-240 Vac $\pm$ 10% Taps must be set at 10 Vac increments.
Phase	1-Phase
Line frequency	60 Hz $\pm$ 2 Hz 50 Hz $\pm$ 2 Hz

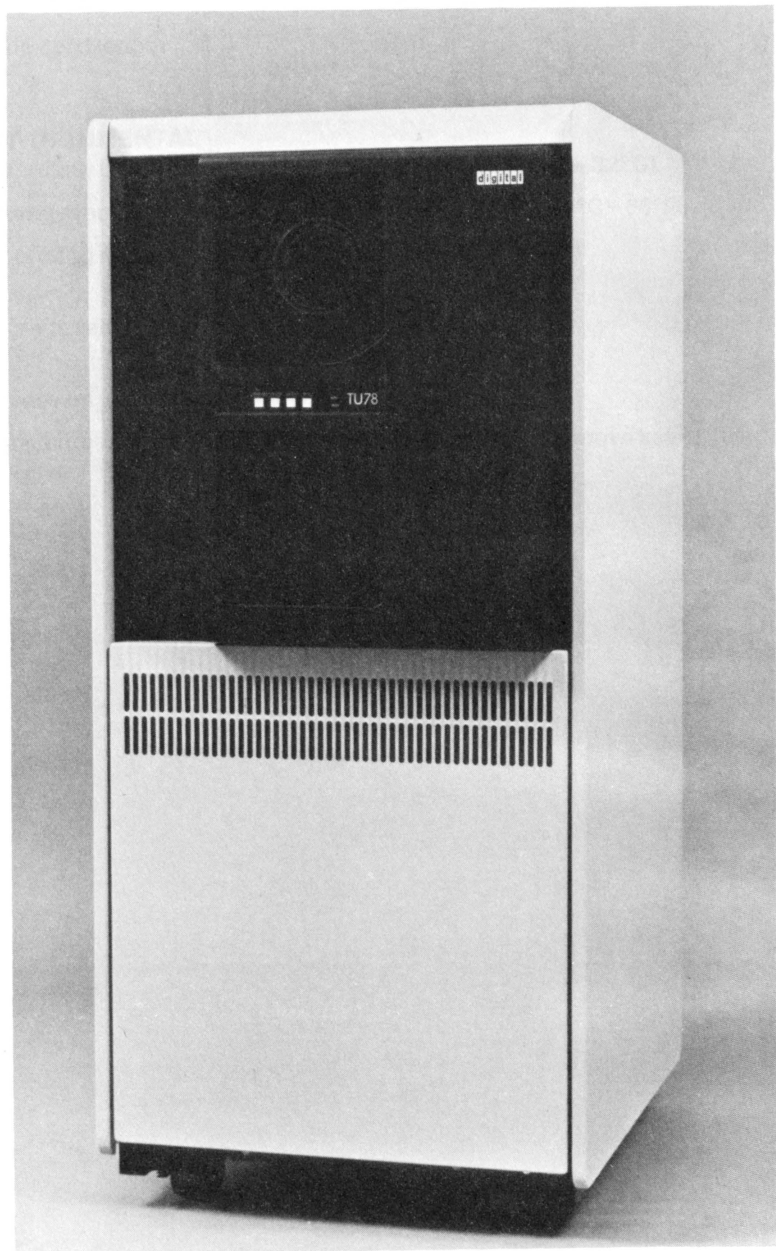
## MAGNETIC TAPES

Receptacle	NEMA #6-20R (240 Vac)
Line cord length	10 ft

### **ENVIRONMENTAL**

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	77°F (25°C)
Maximum operating altitude	8,000 ft (2440 m) above sea level

**MAGNETIC TAPES**



**TU78**

## **TU78**

The TU78 is a 9-track, freestanding, magnetic tape storage system which connects to the processor via the MASSBUS adapter (MBA). The TEU78 subsystems are supported by VAX-11/780 systems only. The TU78 was designed to operate at high speeds in very high usage environments in a wide range of applications, such as fast disk-to-tape backup for large disks, high-speed data acquisition, heavy transaction processing/journaling, tape interchange, and archival storage of large databases.

## **FEATURES**

- Program-selectable recording at 6250 b/in (GCR) or 1600 b/in (PE)
- Read/write speed of 125 in/s
- Automatic tape threading of 10.5 in tape reels as well as IBM Easy Load #1 and #2™ type tape cartridges
- Automatic density select on a READ operation (6250 b/in (GCR) or 1600 b/in)
- Static dual-access capability
- Expandable up to a total of four radially-connected tape transports per subsystem
- Internal microprocessor-controlled diagnostics
- Direct Memory Access (DMA) data transfers
- Vacuum column tape buffering

## **DESCRIPTION**

The TEU78-AB(AD) magnetic tape subsystems consist of a single-access, freestanding tape transport in an H9602 cabinet, a tape formatter and its power supply mounted in the transport cabinet, a MASSBUS adapter (MBA), and a MASSBUS cable. Up to three more add-on TU78-AF(AJ) transports may be added to these subsystems. For those users who already have an MBA, the TU78-AB(AD), consisting of a freestanding tape transport in an H9602 cabinet and a tape formatter and its power supply mounted in the transport cabinet and a MASSBUS cable, is available.

The TEU78-BB(BD) magnetic tape subsystems consist of a dual-access, freestanding tape transport in an H9602 cabinet, a tape formatter and its power supply, two MBAs, and two MASSBUS cables. Up to three more add-on TU78-AF(AJ) transports may be added to these subsystems. Note that dynamic (simultaneous access) dual-port capability of tape subsystems is not supported by DIGITAL operating system software or diagnostics. However, the TEU78-BB(BD) subsystems

tems can be statically shared by two VAX-11/780 processors or connected to one processor through two MBAs for maximum system availability.

### **RECORDING METHODS**

The TU78 writes data in two modes: PE (Phase-Encoded) at 1600 b/in and GCR (Group Coded Recording) at 6250 b/in. Data is written on the tape by magnetizing small sections of the oxide on the tape in different directions, i.e. either positively or negatively. A change or lack of change in the direction between adjacent magnetized sections of tape, depending on the recording method used, indicates whether the bit represented is a 1 or a 0. In PE mode, a change in direction from positive to negative represents a 1 bit and a change in direction from negative to positive represents a 0 bit. In GCR (Group Coded Recording) mode, a change in direction from negative to positive or from positive to negative represents a 1 bit and a lack of change in direction represents a 0 bit. However, the data is specially encoded before it is written onto the tape.

At the beginning of a tape to be written in PE mode, the tape formatter writes a 6 inch identification burst between the BOT marker and the first data record. When writing a record in PE, the tape formatter writes a preamble, the data bytes of the record one by one, a postamble, and then slows the tape down to a stop. The preamble and the postamble are used for synchronizing the data clock circuitry in the tape formatter.

At the beginning of a tape to be written in GCR mode, the tape formatter writes a 6 inch identification burst followed by a 6 inch automatic read amplification (ARA) burst before the first data record. The ARA allows the read amplifiers to automatically adjust to the proper gain when reading a tape. When writing a record in GCR, the tape formatter writes a preamble, the data groups of the record, a resynchronization group (after every 158 data groups), a residual group, a CRC group (Cyclic Redundancy Check), and finally a postamble. The preamble, postamble, and resynchronization groups are used for synchronizing the data clock circuitry in the tape formatter. The residual group contains the data bytes that did not fit into the last data group and the CRC group is used as a final check to ensure that data was read correctly.

### **DATA ORGANIZATION**

The head assembly of a nine-track magnetic tape transport, such as the TU78, consists of one erase head, nine write heads, and nine read heads. The nine read and the nine write heads correspond to the

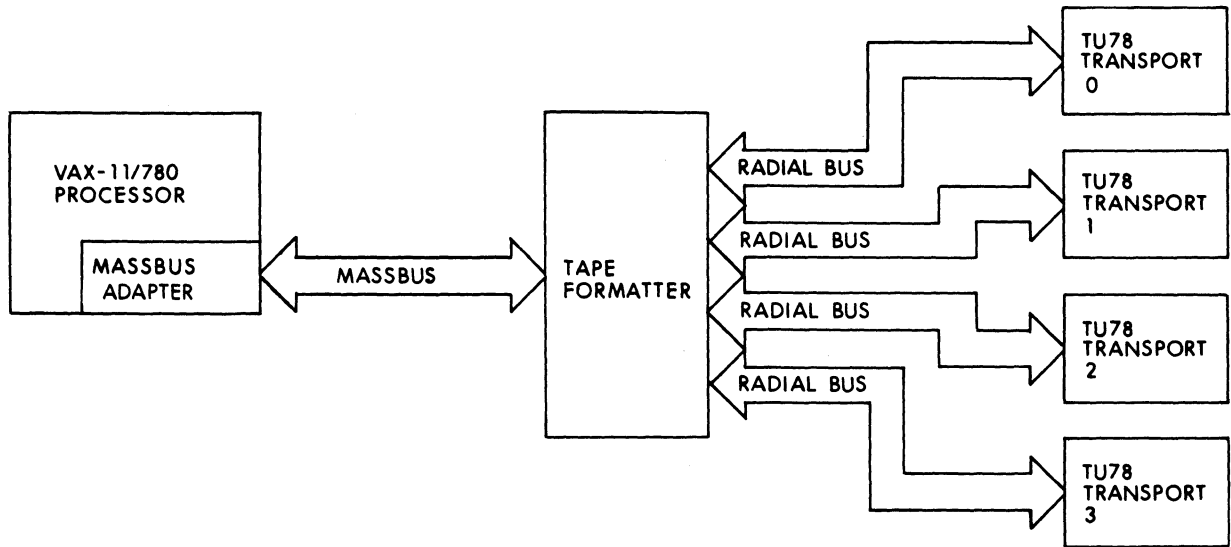


Figure 3-16 TEU78 SYSTEM BLOCK DIAGRAM

lengthwise tracks of the tape, i.e. one read head and one write head for each track. The write head is an electromagnet used to magnetize small sections on the tape. The read head senses flux changes (changes in magnetic direction) on the tape and the erase head erases all information by magnetizing the whole width of the tape all in the same direction.

In order to write the 32-bit data from the processor onto the nine tracks of the TU78, the MBA divides each 32-bit memory word into two 16-bit MASSBUS words. The tape formatter then divides each 16-bit MASSBUS word into two 8-bit bytes and generates a parity bit for each byte. The formatter transfers these 8-bit bytes plus the parity bits to the tape head assembly. Each bit corresponds to one read and one write head, i.e. one track on the tape. Thus, one 8-bit byte of data plus parity is written across the width of the magnetic tape. These data bytes or tape characters, each with its parity bit, are written one at a time in groups called records or blocks. The length of a record is software controlled, but is typically between 12 and 2,000 bytes. The maximum block size allowed by the hardware is 65 KB. In GCR mode, the formatter collects seven of these bytes and then generates an eighth byte called an ECC (Error Checking Character). These eight bytes (a data group) are passed through the formatter's eight-to-ten byte translator, after which the ten bytes plus parity are transferred to the tape head assembly. The tape formatter always stops the tape motion between records leaving an interrecord (IRG) or interblock (IBG) gap of blank tape. This gap is at least 0.6 inches in PE mode and 0.3 inches in GCR mode.

A tape mark is a special short record used by programmers as a software flag. When executing a READ command, the tape formatter will find either data to be read or a tape mark on the tape. When the formatter finds a tape mark, it stops reading the tape and reports the tape mark to the processor by setting the TAPE MARK bit in the drive status register. Usually, one tape mark indicates the end of a file while two tape marks in a row indicate the logical end of the tape.

## **OPERATION**

The TEU78 has eighteen registers plus the MASSBUS adapter registers (Refer to the register section at the back of this book for register diagrams and bit definitions).

Non-data transfer operations such as REWIND, WRITE TAPE MARK, or SPACE FILES can be executed simultaneously by different transports by loading commands into the non-data transfer control registers 0-3 that correspond to transports 0-3. Data transfer opera-



tions such as READ and WRITE can be performed by one transport while other transports execute non-data transfer operations.

Before a READ operation can begin, the processor loads the MBA virtual address, MBA byte counter, tape control, byte count, and control registers, respectively.

The MBA virtual address register specifies the starting memory address of the storage location for the data to be read off the tape. The MBA byte counter register specifies the total number of bytes to be read off the tape and stored in memory. The tape control register specifies how many records are to be read from the tape and selects which of the available transports (up to 4 per formatter) is to perform the READ operation. The byte count register specifies how many bytes each record is expected to contain.

After the MBA virtual address, MBA byte counter, tape control and byte count registers have been loaded, the control register is loaded with the READ command from the processor. The READ command is then executed. An 8-bit byte of data is read off of the tape and then transferred to the formatter which checks the parity. Two 8-bit bytes (one 16-bit word) are stored in the formatter, which generates a parity bit for each 16-bit word. The 16-bit word plus parity is then transferred to the MBA. The MBA combines two 16-bit words into a 32-bit memory word and generates a parity bit. The 32-bit word plus parity is then written into the memory location specified. This process continues until the byte count in the MBA virtual address register or the record count in the tape control register is reached, whichever comes first. When the READ operation is completed, an interrupt is set to alert the processor that the data has been read off the tape.

Before a WRITE operation can begin the processor loads the MBA virtual address, MBA byte counter, tape control, byte count, and control registers respectively.

The MBA virtual address register specifies the starting memory address of the location of the data to be written onto the tape. The MBA byte counter register specifies the total number of words to be written onto the tape. The tape control register specifies how many records are to be written on the tape and selects which of the available transports is to perform the WRITE operation. The byte count register specifies how many bytes each record is to contain.

After the MBA virtual address, MBA byte counter, tape control, and byte count registers have been loaded, the control register is loaded with the WRITE command from the processor. The WRITE command is then executed. A 32-bit word of data is read from memory and

transferred to the MBA which divides the 32-bit word into two 16-bit words and generates a parity bit for each 16-bit word. The MBA then transfers the two 16-bit words plus parity to the formatter. The formatter checks the parity of each 16-bit word and then divides it into two 8-bit bytes and generates a parity bit for each byte. The formatter then writes the two 8-bit bytes plus parity onto the tape one by one. This process continues until the MBA reaches the proper byte count or the formatter reaches the proper record count, whichever comes first. When the operation is completed, an interrupt is set to alert the processor that the data has been written onto the tape.

Other operations include: READ BACKWARD, WRITE TAPE MARK, ERASE GAP, SPACE FORWARD, SPACE BACKWARD, REWIND, REWIND/UNLOAD.

### **DATA INTEGRITY**

Several error checking and correction features of the TU78 ensure that the data has correct parity.

In PE mode, the parity error checking circuitry checks characters one by one during a READ operation. Similarly, the read-after-write circuitry checks characters one by one during a WRITE operation to ensure that the data just written has correct parity. The self-clocking feature allows on-the-fly single-track error correction by detecting and reconstructing lost data during a READ operation.

In GCR mode, the read-after-write parity error circuitry checks characters one by one during a WRITE operation to ensure that the data just written has correct parity. During a READ operation, the formatter holds each eight-byte group in a buffer and checks the parity of each byte. The parity bits and the ECC (Error Checking Character) are used by the error correction circuitry for two-track error correction by reconstructing lost or incorrect data. The CRC group checks to see that data was read off the tape correctly and that any on-the-fly error corrections were performed successfully. During a WRITE operation, the CRC character is generated and written on the tape at the end of each record. During a READ operation the data read is used to generate a second CRC character which is then compared to the CRC read from the end of the record. If there is a discrepancy between the two CRC characters, an error is reported to the processor.

An industry-standard file-protect ring on the tape reel prevents accidental writing on that tape. The operator should remove the ring when the tape reel is stored and insert it only when mounting the tape reel before a WRITE operation.

## INTERRUPTS

The TU78 magnetic tape system MBA uses a vectored interrupt to cause the program to branch to an interrupt service routine. The TU78 generates an interrupt at the completion of an operation, when a error has been detected, or when a transport comes on-line.

## RELIABILITY/MAINTAINABILITY

Reliability means long life expectancy and uninterrupted processing of the magnetic tape system. Special design features of the TU78 magnetic tape systems give them these qualities of high reliability as well as ease of maintenance.

- Easy front access to most assemblies.
- Modular construction of the TU78 enables parts to be quickly removed and replaced during routine servicing and maintenance.
- Integral maintenance keypad and display allow for microprocessor-controlled diagnostics to be performed independent of the host processor.
- On-line microprocessor-controlled diagnostic capability alerts the host processor to microprocessor failure.
- Radial connection from formatter to add-on transports allows independent servicing of transports.

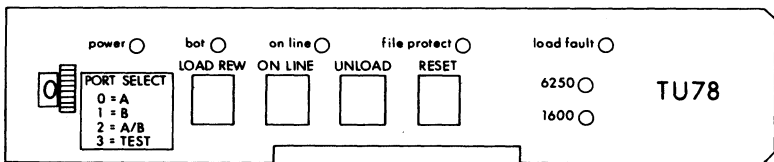


Figure 3-17 TU78 FRONT PANEL CONTROLS AND INDICATORS

## PANEL CONTROLS AND INDICATORS

The front panel controls allow the operator to control the tape transport manually when it is off-line. When on-line, the transport is under program control except for taking it off-line. The indicator lights provide transport status information.

- PORT SELECT switch (thumbwheel on front panel)

When set to 0, selects MASSBUS port A. When set to 1, selects MASSBUS port B. When set to 2, selects both MASSBUS ports A and B. When set to 3, puts the TU78 in Maintenance mode and disables both MASSBUS ports.

## MAGNETIC TAPES

- **LOAD/REWIND switch (momentary pushbutton on front panel)**

Depressing this switch when the tape is not loaded causes the transport to load the tape. Depressing this switch when the tape is loaded causes the transport to rewind the tape to the beginning (BOT). This switch is operational only when the tape transport is off-line.
- **ON-LINE switch (alternate-action pushbutton on front panel)**

Depressing this switch causes the tape transport to go on-line. Depressing it again causes the tape transport to go off-line.
- **UNLOAD switch (momentary pushbutton on front panel)**

Depressing this switch causes the tape transport to rewind and then unload the tape. This switch is operational only when the tape transport is off-line.
- **RESET switch (momentary pushbutton on front panel)**

Depressing this switch terminates all functions and causes the tape transport to go off-line. If the LOAD FAULT indicator is lit, depressing RESET causes it to go out.
- **POWER lamp (red light indicator on front panel)**

When lit, this lamp indicates that the tape transport is turned on.
- **BOT (Beginning Of Tape) lamp (red light indicator on front panel)**

When lit, this lamp indicates that the tape is at BOT.
- **ON LINE lamp (red light indicator on front panel)**

When lit, this lamp indicates that the tape transport is on-line. When not lit, this lamp indicates that the tape transport is off-line because 1) the ON LINE switch has been depressed 2) the processor has issued a REWIND/UNLOAD command 3) a pneumatic failure has been detected or 4) the RESET switch has been depressed.
- **FILE PROTECT lamp (red light indicator on front panel)**

When lit, this lamp indicates that a reel of tape without a file-protect ring has been loaded onto the tape transport.
- **LOAD FAULT lamp (red light indicator on front panel)**

When lit, this lamp indicates that the automatic tape loading mechanism has failed to load the tape after two attempts.
- **6250 lamp (red light indicator on front panel)**

When lit, this lamp indicates that the tape transport is set to read or write at 6250 b/in in GCR mode.
- **1600 lamp (red light indicator on front panel)**

When lit, this lamp indicates that the tape transport is set to read or write at 1600 b/in in PE mode.

**SPECIFICATIONS**

**MECHANICAL**

Cabinet	Freestanding
Controller mounting code (TEU78)	Option panel space
Height	60.5 in (154 cm)
Width	27.5 in (70 cm)
Depth	30 in (76.2 cm)
Weight	560 lbs (254 kg)

**PERFORMANCE**

Transports per formatter	4
Recording density	6250/1600 b/in
Read/write speed	125 in/s
Capacity per 2400 ft reel	
6250 b/in	145 MB with 8 KB records
1600 b/in	40 MB with 8 KB records
Rewind speed	440 in/s
Rewind time	70 s typical per 2400 ft reel
Maximum load time	10 s without a retry
Peak transfer speed	
6250 b/in	780 KB/s
1600 b/in	200 KB/s

**ELECTRICAL**

Starting (surge) current	80 A at 240 Vac
Surge duration	1.2 s
Operating current	13 A at 240 Vac
Power consumption	2295 Watts
Heat dissipation	7826 Btus/hr

## MAGNETIC TAPES

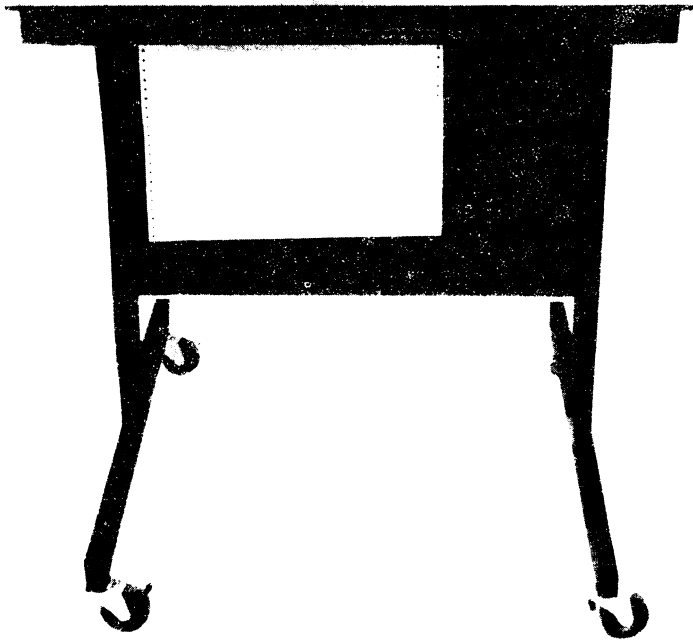
Operating voltage	220-240 Vac $\pm$ 10% Taps must be set at 10 Vac increments.
Phase	1-Phase
Line frequency	60 Hz $\pm$ 3 Hz 50 Hz $\pm$ 3 Hz
Receptacle	Nema #6-30R (240 Vac)
Line cord length	10 ft

### **ENVIRONMENTAL**

Operating temperature	59°F–90°F (15°C–32°C)
Storage temperature	-40°F–151°F (-40°C–66°C)
Operating relative humidity	20%–80% (non-condensing)
Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	77°F (25°C)
Maximum operating altitude	8,000 ft (2440 m) above sea level

### MAGNETIC TAPE TRANSPORTS

	TU58	TS11	TE16	TU77	TU78
<b>READ/WRITE SPEED</b>	30 in/s	45 in/s	45 in/s	125 in/s	125 in/s
<b>RECORDING DENSITY</b>	800 b/in	1600 b/in	800/1600 b/in	800/1600 b/in	1600/6250 b/in
<b>TAPE THREADING</b>	N/A	MANUAL	MANUAL	AUTOMATIC	AUTOMATIC
<b>REWIND TIME</b>	N/A	2 min PER REEL	3.7 min PER REEL	65s PER REEL	65s PER REEL
<b>OFF-LINE DIAGNOSTICS</b>	N/A	YES	NO	NO	YES
<b>MEDIA TYPE</b>	CASSETTE CARTRIDGE	½ in TAPE REEL-TO-REEL	½ in TAPE REEL-TO-REEL	½ in TAPE REEL-TO-REEL	½ in TAPE REEL-TO-REEL
<b>NO. OF TRACKS</b>	2	9	9	9	9
<b>STORAGE CAPACITY (8 KB BLOCKS)</b>	262 KB PER CARTRIDGE	40 MB PER REEL	40 MB PER REEL	40 MB PER REEL	145 MB PER REEL
<b>PEAK TRANSFER SPEED</b>	3.7 KB/s	72 KB/s	72 KB/s	200 KB/s	780 KB/s
<b>TAPE BUFFERING</b>	N/A	TENSION ARM	VACUUM COLUMN	VACUUM COLUMN	VACUUM COLUMN
<b>TRANSPORTS PER FORMATTER</b>	2 (only one works at a time)	1	8	4	4



LXY11.21



## CHAPTER 4

# LINEPRINTERS

### LXY11/21

The LXY11 and the LXY21 are freestanding, dot matrix lineprinter/plotters connected to the UNIBUS via the controller. The LXY11-A(B), LXY11-E(F), LXY11-H(J), LXY21-A(B), LXY21-E(F), and LXY21-H(J) versions are supported by UNIBUS PDP-11 systems. The LXY11-S(T) and the LXY21-S(T) versions are supported by VAX-11/780 systems while the LXY11-V(W) and the LXY21-V(W) versions are supported by VAX-11/750 systems. The LXY11/LXY21 lineprinter/plotters are especially suited for operation in the scientific, engineering, industrial, and commercial marketplaces.

### FEATURES

- Printing and plotting capabilities
- Superior print quality due to overlapping dots
- Standard Programmable Vertical Forms Unit (PVFU)
- Multipart forms printing capability

### DESCRIPTION

The LXY11 and the LXY21 are versatile printing devices that combine the benefits of a dot matrix printer and a plotter.† The LXY11/LXY21 systems consist of a freestanding lineprinter/plotter unit, a controller, and a 25 ft (7.6 m) cable for connecting the controller to the printer/plotter. The LXY11 produces high quality output at speeds up to 300 l/min for printing and up to 16.7 in/min for plotting. The LXY21 is a higher speed device which prints at up to 600 l/min and plots at up to 33.3 in/mjn.

The PLXY-11 graphics software package provides the LXY11/LXY21 lineprinter with its unique plotting capabilities. The LXY11/LXY21 printer/plotter systems can plot standard line drawings (graphs, histograms, charts, etc.) as well as plots requiring shaded or solid areas (bar graphs, bar codes, large, solid characters, etc.). This capability is particularly useful in industrial and distributive applications where products must be coded and labeled using pre-printed stationery, gummed labels, etc. Explanatory text or large, solid characters for labeling may be incorporated where desired.

† See Appendix B for examples of actual print copy and graphics.

Because the LXY11/LXY21 printer/plotter systems print overlapping dots anywhere on a page, plots are always sharp and uniformly dense. Note that complex, intricate plots print just as quickly as simple designs and that the LXY11/LXY21 systems are ideally suited to provide hardcopy output of designs formulated on a graphics terminal.

The LXY11/LXY21 prints the full 96-character ASCII set as well as double-height characters and underlines. A choice of six or eight lines to the inch (selected by the operator or under program control) is standard on both devices. Line lengths of up to 132 characters and any length of form up to 22 inches at 6 l/in (14.5 inches at 8 l/in) can be printed. Both the LXY11 and the LXY21 print on single-part or multi-part forms of continuous fanfold edge-perforated paper. Up to six copies of multipart forms can be produced.

Both the LXY11 and the LXY21 dot matrix printer/plotters are constructed with a minimum of moving parts and utilize simple hammer drive circuitry. The LXY11 hammer bank has 44 hammers while the LXY21 print mechanism has 66. Each hammer prints a single dot. The hammer bank shuttles back and forth sweeping 3-character (36 dot) positions on the LXY11 and 2-character (24 dot) positions on the LXY21. The hammers print dense overlapping dots of .020 in in diameter on a dot matrix of 9X7 dots (or 9X9 dots for lower case letters with descenders) anywhere on a page. The 9X7 matrix enables the printer to overlap dots both horizontally and vertically resulting in solid-looking characters and lines produced clearly with uniform density.

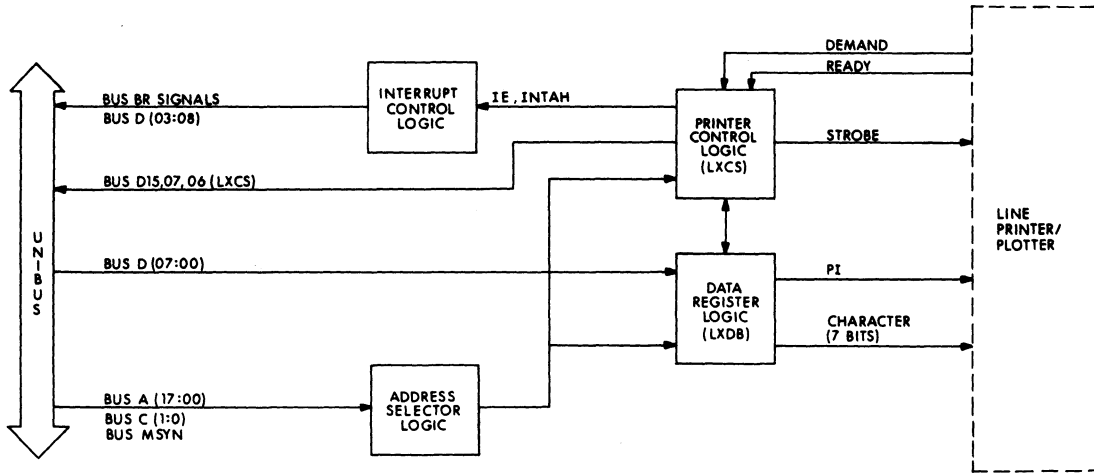
### OPERATION

The LXY11 and the LXY21 have two internal registers: the Control and Status Register (LXCS) and the Data Buffer Register (LXDB). (Refer to the lineprinter register section in the back of this book for the LXCS and LXDB diagrams.)

When the READY bit in the control and status register is set, the printer/plotter is ready to accept a character from the processor.

The processor loads characters one by one into the data buffer register in the controller. The controller then transfers the characters to a 132 character data buffer in the printer/plotter. The line length of 132 characters corresponds directly to this 132 character data buffer.

The current data buffer register (LXDB) contents are automatically printed out whenever either of the two control codes (Line Feed, Form Feed) is recognized. The Line Feed (LF) code advances the paper one line while the Form Feed (FF) code advances the paper to the top of the next page. If neither of these control codes is recognized, the



LINEPRINTERS

Figure 4-1 LXY11/21 SYSTEM BLOCK DIAGRAM

contents of the data buffer will automatically be printed out when it is full.

An Elongate code ( $010_8$ ) anywhere in a line of characters, causes the entire line to be printed double-height. To underline certain characters in a line, a Carriage Return (CR) code ( $015_8$ ) is sent following the line of characters, which causes the lineprinter to wait for a line of control characters specifying which of the characters in the line already sent are to be underlined. Unlike the Elongate code which causes an entire line to be printed double-height, the Carriage Return code causes only those characters specified to be underlined.

The Programmable Vertical Format Unit (PVFU) allows the user, under program control, to skip to a preselected line (Vertical Tab Stop) on a form. Forms may be as long as 132 lines and 13 different Vertical Tab Stops are available, although the same Vertical Tab Stop number may be assigned to more than one line at a time.

A Plot Mode code ( $005_8$ ) anywhere in a line of characters causes the lineprinter to plot the entire line instead of print. When plotting, only one row of dots is printed at a time and the paper advances only one dot row with each Line Feed code ( $012_8$ ). The characters are printed as a stream of binary bits, i.e. each 1 bit prints as a dot and each 0 bit prints as a blank dot space.

## **SPECIAL NON-PRINTING ASCII CONTROL CODES‡**

### **ELONGATE ( $010_8$ )**

The Elongate code sent anywhere in a line of characters, causes the entire line to be printed double-height.

### **CARRIAGE RETURN ( $015_8$ )**

The Carriage Return code is used for underlining. It causes the lineprinter to wait for a line of control code characters (Underline, Delete, or Space) before printing out the line of characters already in the data buffer register. Each control code character sent corresponds to a data character currently in the data buffer register. An Underline ( $137_8$ ) control code character causes the lineprinter to underline the corresponding data character. A Delete ( $177_8$ ) control code character causes the lineprinter to replace the corresponding data character with a blank space and a Space ( $040_8$ ) control code character causes the lineprinter to print the corresponding data character unchanged.

‡ See Appendix C for ASCII code chart.

**SHIFT OUT (016<sub>8</sub>)**

The Shift Out code causes all subsequent characters to be selected from the optional character set on the PROM currently in use.

**SHIFT IN (017<sub>8</sub>)**

The Shift In code causes all subsequent characters to be selected from the ASCII character set. A Shift In is automatically generated at the end of every line.

**SHIFT TO 8 LPI (006<sub>8</sub>)**

The Shift to 8 LPI code causes the next Line Feed code (012<sub>8</sub>) to advance the paper one-eighth of an inch for 8 lines/in spacing instead of the standard 6 lines/in. The lineprinter automatically resets itself to 6 LPI after the Line Feed operation. Shift to 8 LPI is only operational when the 8 LPI switch on the lineprinter is set to 6 LPI.

**PLOT MODE (005<sub>8</sub>)**

The Plot Mode code sent anywhere in a line of characters causes the lineprinter to plot the entire line instead of printing ASCII characters. There are 1583 dot positions across the width of the paper, i.e. 12 dot positions for each of the 132 characters. Plot Mode allows the printing of only the odd-numbered dots or 6 dots per character. Bits <0-5> of each character correspond to the 6 printable dots of that character space. The characters are printed as a stream of binary bits, i.e. each 1 bit prints as a dot and each 0 bit prints as a blank dot space. For instance, printing 101<sub>8</sub> (01 000 001<sub>2</sub>) causes only dot number 1 to be printed for that character; printing 1028 (01 000 010) prints dot number 3; and printing 055<sub>8</sub> (00 101 101<sub>2</sub>) prints dot numbers 1,5,7, and 11. Codes 100<sub>8</sub>-137<sub>8</sub> must be used instead of codes 000<sub>8</sub>-037<sub>8</sub>, which cannot be used to plot data because they are control codes and will be interpreted as such, i.e. Line Feed (012<sub>8</sub>).

**DOUBLE DENSITY PLOT MODE (004<sub>8</sub>)**

The Double Density Plot Mode (DDPM) code allows printing of all of the even dot positions. A DDPM code sent anywhere in a line of characters causes the lineprinter to plot the entire line instead of printing ASCII characters. Double Density Plot Mode allows the printing of only the even-numbered dots or 6 dots per character. Note that the Line Feed code at the end of a line of characters does not cause the paper to advance. The DDPM code must always be followed by a Plot Mode Code (005<sub>8</sub>), which fills in all of the odd-numbered dot positions.

### **START LOAD (036<sub>g</sub>)**

The Start Load code initializes the PVFU and causes all subsequent characters to be loaded into the PVFU buffer.

### **STOP LOAD (037<sub>g</sub>)**

The Stop Load code indicates the end of the characters to be loaded into the PVFU buffer. The PVFU buffer allows storage of a Vertical Tab Stop code (channel) for each line of the form. Forms may be up to 132 lines long. Vertical Tab Stops are codes 020<sub>g</sub>-035<sub>g</sub>. A Vertical Tab Stop code sent anywhere in a line of characters causes the paper to advance to the next PVFU line indicated by that Vertical Tab Stop code at the next Line Feed code. Top of Form code 020<sub>g</sub> is always loaded into line 1 in the PVFU buffer.

### **INTERRUPTS**

The LX11/LX21 system controller uses bus request (BR) interrupts to gain control of the UNIBUS to perform a vectored interrupt, which causes the program to branch to a handling routine. A BR interrupt can occur only if the INTERRUPT ENABLE bit in the control and status register is set. Once INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the READY or ERROR bit in the control and status register is set.

When the READY bit is set, the printer/plotter is ready to accept a character to be loaded into the data buffer register (LXDB). When the ERROR bit is set, it indicates that some error condition exists. In this case, an interrupt is generated to cause the program to branch to an error handling routine.

The interrupt priority level is 4 and the interrupt vector address is 200. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy, high quality output, and continuous smooth processing of the lineprinter system. Special design features of the LX11 and the LX21 lineprinter systems give them these qualities of high reliability as well as ease of maintenance.

- The LX11 and the LX21 use hammer bank print mechanisms and are therefore not susceptible to the wear of single head matrix printers.

## LINEPRINTERS

- The hammers never require adjustment or alignment. The hammer bank module can be easily removed since it is held in place by only two screws.
- Less chance of paper jams than with charaband printers since the paper moves as it prints. As the paper advances each successive line of dots overlaps to form solid-looking characters.
- Fewer moving parts than charaband and drum printers and 50% fewer components than mechanical font printers.
- Modular construction enables parts to be quickly removed and replaced during routine servicing and maintenance.
- The LXY11 and the LXY21 freestanding unit is designed to give stable, quiet operation below 65 dB.

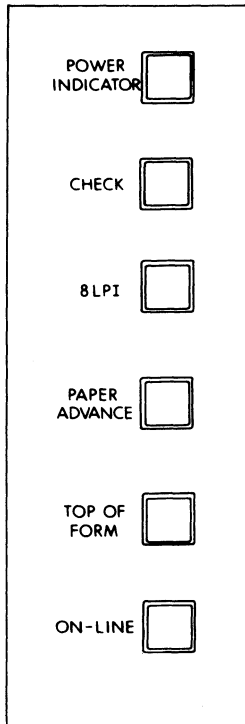


Figure 4-2 LXY11/21 FRONT PANEL CONTROLS AND INDICATORS

## PANEL CONTROLS AND INDICATORS

The front panel controls allow the operator to control the printer/plotter manually while the internal controls allow the operator to position the paper. The indicator lights provide printer/plotter status information.

- **POWER switch** (2-position toggle switch located on the base panel at the left-hand end of the printer/plotter and associated white light indicator on front panel)

This switch controls application of all power to the printer/plotter. When set to ON, power is applied to the printer/plotter causing the associated indicator to light. When set to OFF, power is removed from the printer/plotter causing the associated indicator light to go out.

- **CHECK switch** (momentary pushbutton/red light indicator switch on front panel)

When lit, this switch indicates an error condition such as paper not loaded properly, paper jam, paper shortage, torn paper, abnormal supply voltages, cover left open, or Form Thickness Adjust lever left up. To resume normal on-line operation requires operator intervention. The CHECK light will automatically go out once the error has been corrected except when loading paper. After reloading paper, the operator must press the CHECK pushbutton again and the indicator light will go out.

- **8 LPI switch** (momentary pushbutton/white light indicator switch on front panel)

When lit, this switch indicates line spacing of 8 lines per inch. When not lit, it indicates line spacing of 6 lines per inch. Line spacing may also be selected under program control. However, if 8 LPI has been selected off-line (indicator not lit), the controller cannot select 6 LPI on-line. On the other hand, if 6 LPI has been selected off-line (indicator lit), the controller can select either 6 or 8 LPI on-line. This switch is operational only when the printer/plotter is off-line.

- **PAPER ADVANCE switch** (momentary pushbutton on front panel)

While depressed, this switch causes the paper to advance at slew rate.

- **TOP OF FORM switch** (momentary pushbutton on front panel)

When depressed, this switch causes the paper to advance to the top of the next form or to the Top of Form specified by the PVFU, if loaded. This switch is operational only when the printer/plotter is off-line.



- **ON-LINE** switch (momentary pushbutton/white light indicator switch on front panel)

When lit, this switch enables the printer/plotter controller. When not lit, it disables the controller. The printer/plotter cannot go on-line if the CHECK indicator is lit.

Internal controls: Forms Thickness Adjustment, Horizontal Form Position Adjustment, and Vertical Form Position Adjustment.

## **SPECIFICATIONS**

### **MECHANICAL**

Cabinet	Freestanding
Controller mounting code	One quad slot
Height	40.5 in (103 cm)
Width	30 in (76.2 cm)
Depth	24.3 in (61.6 cm)
Weight	210 lbs (95.3 kg)

### **PERFORMANCE**

#### Printing Speed

LXY11	300 l/min
LXY11	240 l/min for underlines or lower case characters with descenders
LXY11	162 l/min for double-height characters
LXY11	131 l/min for double-height characters with descenders or underlines
LXY21	600 l/min
LXY21	465 l/min for underlines or lower case characters with descenders
LXY21	323 l/min for double-height characters

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LXY21 265 l/min for double-height characters with descenders or underlines

### Plotting Speed

LXY11 16.7 in/min

LXY11 8.3 in/min for double density plotting

LXY21 33.3 in/min

LXY21 16.7 in/min for double density plotting

### Paper Slew Speed

LXY11 8 in/sec (20.3 cm/sec)

LXY21 16 in/sec (40.6 cm/sec)

## ELECTRICAL

Interface (controller) current 1.5 at +5 Vdc

Power consumption 450 Watts

Heat dissipation 1535 Btus/hr

Operating voltage 120 Vac  $\pm$  10%  
240 Vac  $\pm$  10%

Phase 1-Phase

Line frequency 60 Hz  $\pm$  3 Hz  
50 Hz  $\pm$  3 Hz

Receptacles Nema #5-15R (120 Vac), Nema #6-15R (240 Vac)

Line cord length 10 ft (3 m)

## ENVIRONMENTAL

Operating temperature 50°F–100°F (10°C–38°C)

Storage temperature -40°F–149°F (-40°C–65°C)

Operating relative humidity 30%–90%  
(non-condensing)

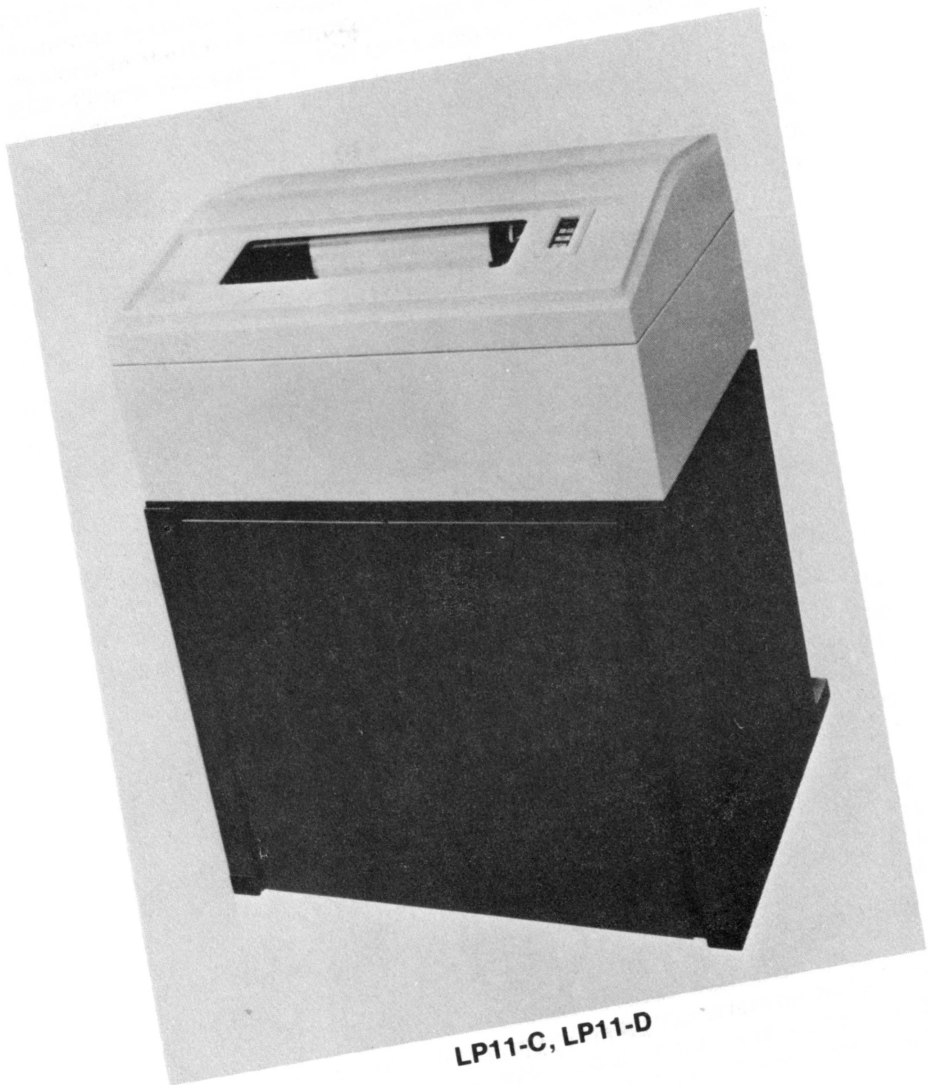
Storage relative humidity 5%–95%  
(non-condensing)

Maximum operating altitude 7,500 ft (2288 m) above sea level

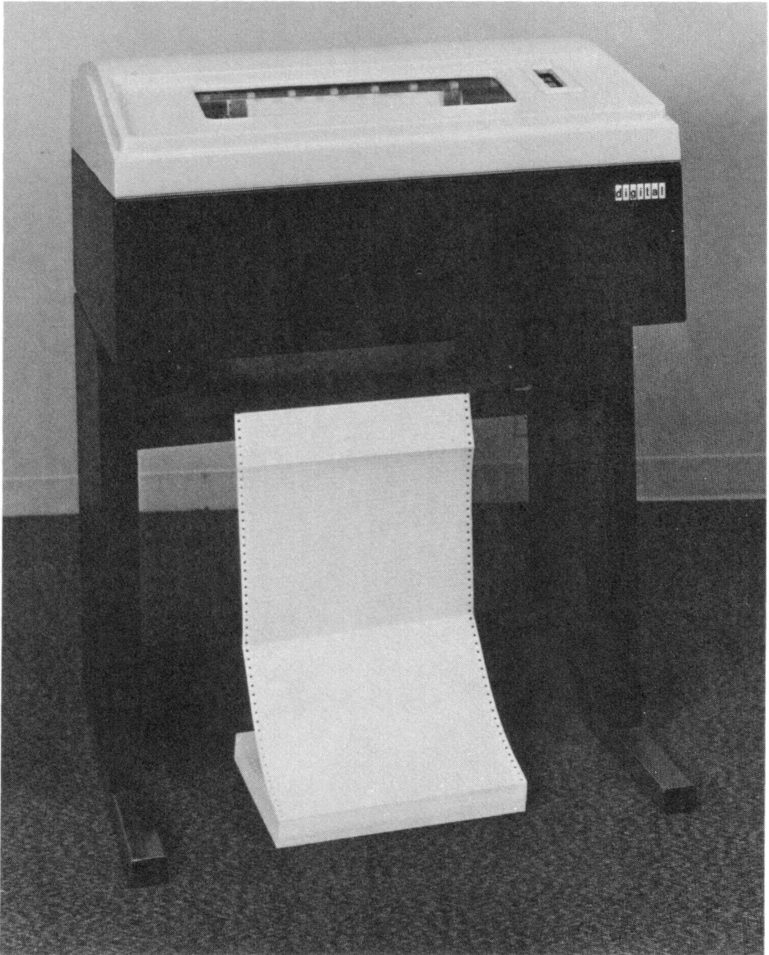




**LP11-A, LP11-B, LP11-E**



LP11-C, LP11-D



**LP11-Y, LP11-Z**

## LP11 SERIES

The LP11-A(B), LP11-E, LP11-C(D), and LP11-Y(Z) are freestanding lineprinter systems connected to the UNIBUS via the controller. All versions of the LP11 lineprinter system are supported by UNIBUS PDP-11 and VAX systems. The LP11-A(B) versions are band printers designed to operate at low speeds while the LP11-E versions are band printers designed to operate at medium speeds, both in moderate usage environments. The LP11-C(D) and the LP11-Y(Z) versions are medium speed drum printers designed to operate in moderate usage environments. All LP11 lineprinters are suitable for a wide range of applications including the commercial, scientific, educational, and industrial marketplaces.

## FEATURES

- Heavy-duty construction
- Optional Programmable Vertical Forms Unit (LP11-Y(Z) only)
- Wide selection of optional character sets (band lineprinters only)
- Interchangeability of character sets (band lineprinters only)
- Multipart forms printing capability

## DESCRIPTION

The LP11-A(B) band lineprinter systems consist of a freestanding lineprinter unit, a controller, a 30 ft (9.2 m) cable for connecting the controller to the lineprinter, and a universal power supply. The LP11-AA prints at speeds up to 300 l/min using a 64-character ASCII set while the LP11-BA prints at speeds up to 300 l/min using a 64-character ASCII set and 215 l/min using a 96-character ASCII set.

The LP11-EA(EB) band lineprinter systems consist of a freestanding lineprinter unit, a controller, and a 30 ft (9.2 m) cable for connecting the controller to the lineprinter. The LP11-EA prints at speeds up to 600 l/min using a 64-character ASCII set while the LP11-EB prints at speeds up to 600 l/min using a 64-character ASCII set and 445 l/min using a 96-character ASCII set.

A band is a flat, steel belt with raised metal characters on the face. The band is mounted on two pulleys—one to the right and one to the left of the paper. The LP11-E hammer bank has 132 hammers (one for each

column), while the LP11-A(B) hammer bank has only 66 hammers (each two columns wide). When the selected character in a column comes around on the moving band, the corresponding hammer strikes it. On the LP11-E versions, as the band moves past the paper every hammer strikes one character, thus printing a line. However, on the LP11-A(B) versions, there is a blank space beside each character on the band so that when the two column wide hammer strikes, it prints only one character. Therefore, on the LP11-E versions, every hammer must strike only once to print a line while on the LP11-A(B) versions every hammer must strike twice to print a line.

A wide selection of optional character styles (fonts) is available including foreign languages and a compressed printing mode (available on the LP11-A(B) versions only). The character sets are contained on bands which may be changed by the user.

A drum is a large metal cylinder with 132 columns of raised characters encircling it. The LP11-C(D) and the LP11-Y(Z) hammer bank has 132 hammers (one for each column). When the selected character in a column comes around on the rotating drum, the corresponding hammer strikes the character. During the course of each drum revolution every hammer strikes one character, thus printing a line.

The LP11-C(D) drum lineprinter systems consist of a freestanding lineprinter unit, a controller, and a 25 ft (7.6 m) cable for connecting the controller to the lineprinter. The LP11-CA(CD) prints at speeds up to 900 l/min using a 64-character ASCII set while the LP11-DA(DD) prints at speeds up to 660 l/min using a 96-character ASCII set.

The LP11-Y(Z) drum lineprinter systems consist of a freestanding lineprinter unit, a controller, and a 25 ft (7.6 m) cable for connecting the controller to the lineprinter. The LP11-YA(YD) prints at speeds up to 600 l/min using a 64-character ASCII set while the LP11-ZA(ZD) prints at speeds up to 436 l/min using a 96-character ASCII set.

The LP05K-LL, a long-line interface, is available from Computer Special Systems (CSS) as an option for remote installations. It allows up to 2,000 ft (610 m) between the lineprinter and the host processor.

All versions of the LP11 lineprinter print on single-part or multipart forms of continuous fanfold edge-perforated paper. Up to six copies of multipart forms can be produced.

## **OPERATION**

The LP11 has two internal registers: the Control and Status Register (LPCS) and the Data Buffer Register (LPDB). (Refer to the lineprinter register section in the back of this book for the LPCS and LPDB diagrams.)



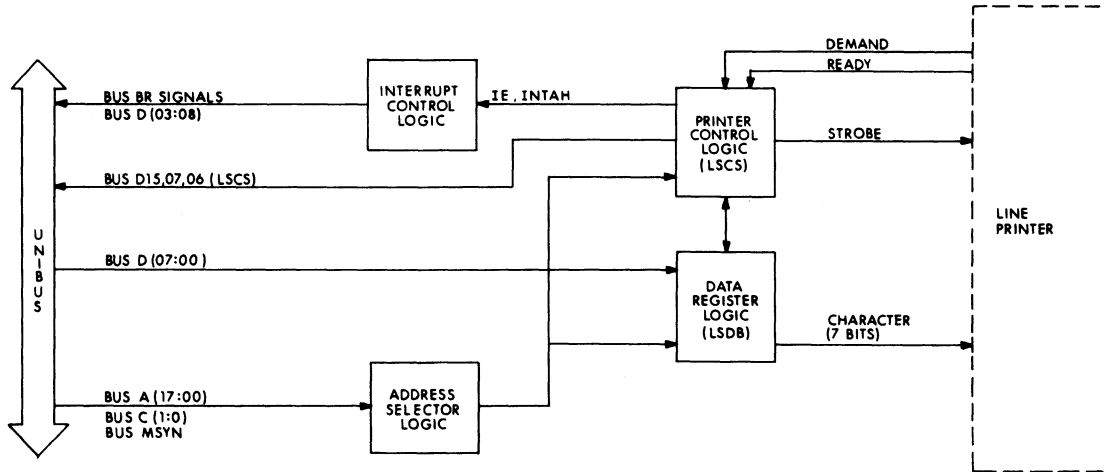


Figure 4-3 LP11 SYSTEM BLOCK DIAGRAM

When the READY bit in the control and status register is set, the lineprinter is ready to accept a character from the processor.

The processor loads characters one by one into the data buffer register in the controller. The controller then transfers the characters to a 132-character data buffer in the printer/plotter. The line length of 132 characters corresponds directly to this 132-character data buffer.

The current data buffer register (LPDB) contents are automatically printed out whenever any of the three ASCII control codes (Line Feed, Form Feed, Carriage Return) is recognized.† The Line Feed (LF) code advances the paper one line, the Form Feed (FF) code advances the paper to the top of the next page, and the Carriage Return (CR) code prints the line but does not advance the paper.

The Programmable Vertical Forms Unit (PVFU) is available as an option for the LP11-Y(Z) versions. It allows the user, under program control, to skip to a preselected line (Vertical Tab Stop) on a form. Forms may be as long as 143 lines and 12 different Vertical Tab Stops (channels) are available. One or more Vertical Tab Stops are assigned to each line so that the same Vertical Tab Stop may be assigned to more than one line at a time. The Start Load command ( $356_8$ ) initializes the PVFU and causes all subsequent characters to be loaded into the PVFU buffer. The Stop Load command ( $357_8$ ) indicates the end of the characters to be loaded into the PVFU buffer. The PVFU buffer allows storage of two characters for each line of the form. The PVFU only uses the low-order 6 bits of each character. The 12 bits (2 characters) stored per line in the PVFU correspond to the 12 Vertical Tab Stops. A 1 bit in a bit position in one of these two characters assigns a Vertical Tab Stop to that line. Bits <0-5> of the first characters correspond to Vertical Tab Stops 1-6 while bits <0-5> of the second character correspond to Vertical Tab Stops 7-12. Vertical Tab Stops are commands  $200_8$ - $213_8$ . A Vertical Tab Stop command sent anywhere in a line of characters causes the paper to advance to the next PVFU line indicated by that Vertical Tab Stop command at the next Line Feed code. Line 1 is assigned to Vertical Tab Stop 1 and the last line of the form is assigned to Vertical Tab Stop 12. Sending command  $200_8$  causes the paper to advance to the top of the next form. Commands  $201_8$ - $212_8$  correspond to Vertical Tab Stops 2-11 and cause the paper to advance to the next line that is loaded with that Vertical Tab Stop. Command  $213_8$  causes the paper to advance to the bottom of the form.

† See Appendix C for ASCII code chart.

## **INTERRUPTS**

The LP11 controller uses bus request (BR) interrupts to gain control of the UNIBUS to perform a vectored interrupt, which causes the program to branch to an interrupt service routine. A BR interrupt can occur only if the INTERRUPT ENABLE bit in the control and status register is set. Once INTERRUPT ENABLE bit is set, an interrupt request is generated whenever either the READY or ERROR bit in the control and status register is set.

When the READY bit is set, the lineprinter is ready to accept the next character to be loaded into the data buffer register (LPDB). When the ERROR bit is set, it indicates that some error condition exists. In this case, an interrupt is generated to cause the program to branch to an error handling routine.

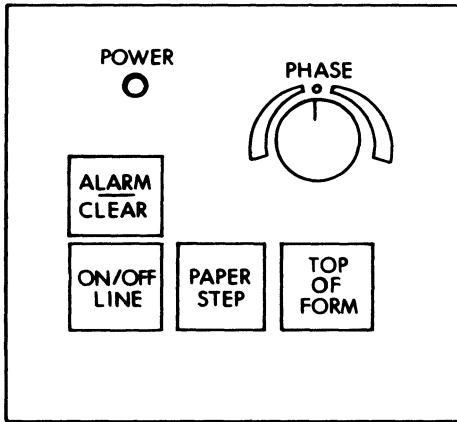
The interrupt priority level is 4 and the interrupt vector address is 200. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## **RELIABILITY/MAINTAINABILITY**

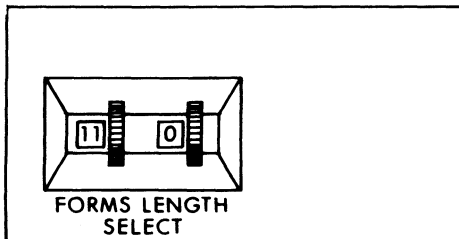
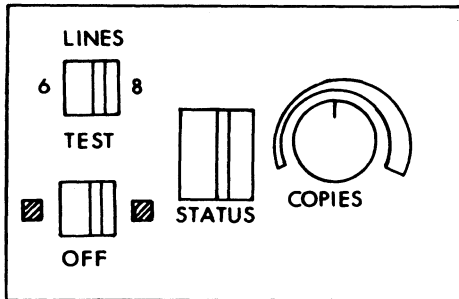
Reliability means long life expectancy, high quality output, and continuous smooth processing of the lineprinter system. Special design features of the LP11 series lineprinter systems give them these qualities of high reliability as well as ease of maintenance.

- The LP11 lineprinter systems require infrequent repairs and adjustments due to their heavy-duty construction.
- All LP11 lineprinter systems have built-in self-test capabilities.
- Modular construction enables parts to be quickly removed and replaced during routine servicing and maintenance.
- The LP11-C(D) freestanding unit is designed to give stable, quiet operation below 65dB.

LINEPRINTERS



FRONT PANEL



UNDER CONSOLE COVER

Figure 4-4 LP11-A(B), LP11-E CONTROLS AND INDICATORS

## CONTROLS AND INDICATORS

The front panel controls and those located under the console cover allow the operator to control the lineprinter manually. The internal controls allow the operator to position the paper. The indicator lights provide the operator with lineprinter status information.

### LP11-A(B), LP11-E CONTROLS AND INDICATORS

- POWER ON/OFF switch (rocker switch located on the front of the lineprinter below the front panel/associated green light indicator on front panel)

This switch controls application of all power to the lineprinter. When set to ON, power is applied to the lineprinter causing the associated indicator to light. When set to OFF, power is removed from the lineprinter causing the associated indicator light to go out.

- ON/OFF LINE switch (alternate-action pushbutton/green light indicator on front panel)

Depressing this switch causes the lineprinter to go on-line and the indicator light to go on. Depressing it again causes the lineprinter to go off-line and the indicator light to go out providing that the lineprinter data buffer is empty.

- ALARM/CLEAR switch (momentary pushbutton/red light indicator on front panel)

When the ALARM/CLEAR indicator is lit an error condition exists in the lineprinter. The code shown by the STATUS display identifies the specific error. To resume normal on-line operations requires operator intervention.

- PAPER STEP switch (momentary pushbutton on front panel)

When depressed, this switch causes the paper to advance one line. This switch is operational only when the lineprinter is off-line.

- TOP OF FORM switch (momentary pushbutton on front panel)

When depressed, this switch causes the paper to advance to the top of the next form specified by the Forms Length Selector switch. This switch is operational only when the lineprinter is off-line.

- PHASE control (vernier on front panel)

This control adjusts the hammer phasing and is used to achieve equal printing density on the left and right sides of each character.

- **6/8 LINES (per inch) switch (2-position toggle switch under console cover)**

When set to 6, this switch indicates line spacing of 6 lines per inch. When set to 8, it indicates line spacing of 8 lines per inch. This switch must be reset by depressing the Top of Form switch.

- **TEST switch (3-position toggle switch under console cover)**

When this switch is set to the center or OFF position, the self-test function is disabled. The lineprinter is set in this position during normal on-line operation. When the lineprinter is off-line and this switch is set to the lefthand position, a fixed vertical pattern is printed, i.e. all 132 character positions print a capital H. When the lineprinter is off-line and this switch is set to the righthand position, a sliding pattern is printed, i.e. all 132 character positions print the entire band pattern shifting one character position to the left after each line. When this switch is set to the center position while the lineprinter is printing either a fixed vertical or sliding pattern, one line of each character on the band will be printed.

- **STATUS display (alphanumeric display under the console cover)**

The code shown by this display identifies one of 45 possible error conditions, when an error condition is indicated by the ALARM/CLEAR indicator light. When no error condition exists, code (77) indicating normal on-line operation appears on the display.

- **COPIES control (vernier under console cover)**

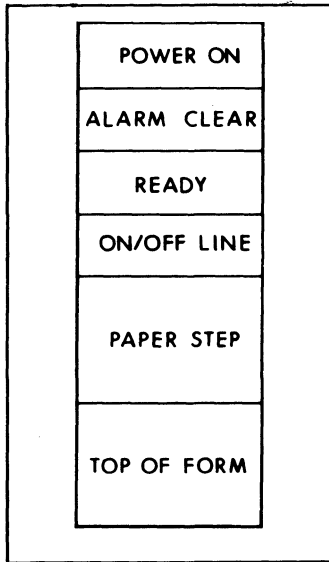
This control adjusts the force of hammer impact when printing multiple copies.

- **FORMS LENGTH SELECTOR switch (2 thumbwheels under console cover)**

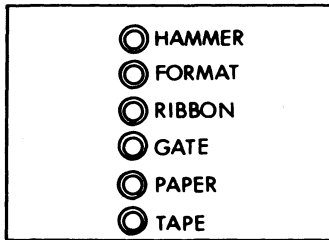
This selector sets the form length from 3 in to 14.75 in. This switch must be reset by depressing the Top of Form switch.

Internal controls: Horizontal Form Position Adjustment and Vertical Form Position Adjustment (sprocket locks).

LINEPRINTERS



FRONT PANEL



UNDER CONSOLE COVER

Figure 4-5 LP11-C(D), LP11-Y(Z) CONTROLS AND INDICATORS

## LP11-C(D), LP11-Y(Z) CONTROLS AND INDICATORS

- **POWER ON/OFF switch** (2-position toggle switch located on the front of the lineprinter below the front panel/associated green light split indicator on front panel)

This switch controls application of all power to the lineprinter. When set to ON, power is applied to the lineprinter causing the associated indicator to light. When set to OFF, power is removed from the lineprinter causing the associated indicator light to go out.
- **ALARM/CLEAR switch** (momentary pushbutton/red light split indicator on front panel)

When the ALARM/CLEAR indicator is lit, one or more of the following red light fault indicators is also lit: HAMMER, FORMAT, RIBBON, GATE, PAPER, or TAPE. To resume normal on-line operations requires operator intervention.
- **READY/ON/OFF LINE switch** (alternate-action pushbutton/white light split indicator on front panel)

When the READY half of the split indicator is lit, the lineprinter is ready to be put on-line. Depressing the switch causes the ON/OFF LINE half of the split indicator to light indicating that the lineprinter is on-line and under program control. Depressing the switch again causes the ON/OFF LINE half of the split indicator to go out indicating that the lineprinter is off-line providing that the lineprinter data buffer is empty.
- **PAPER STEP switch** (momentary pushbutton on front panel)

When depressed, this switch causes the paper to advance one line. This switch is operational only when the lineprinter is off-line.
- **TOP OF FORM switch** (momentary pushbutton on front panel)

When depressed, this switch causes the paper to advance to the top of the next form. This switch is operational only when the lineprinter is off-line.
- **HAMMER fault** (red light indicator under console cover)

When lit, this indicator warns of a HAMMER fault and causes the lineprinter to go off-line after printing the current line and the ALARM indicator to light. To resume normal on-line operations requires the operator to turn the power off and then on again.
- **FORMAT fault** (red light indicator under console cover)

When lit, this indicator warns that the Vertical Forms Unit is on the wrong line and causes the lineprinter to go off-line after printing the current line and the ALARM indicator to light. Cleared by depressing the Forms Reset toggle switch.



- RIBBON fault (red light indicator under console cover)

When lit, this indicator warns that the ribbon direction has failed to reverse at the end of a spool or that a ribbon snag has developed. A RIBBON fault causes the lineprinter to go off-line after printing the current line and the ALARM indicator to light. To resume normal on-line operations requires operator intervention.

- GATE fault (red light indicator under console cover)

When lit, this indicator warns that the drum gate is open and causes the lineprinter to go off-line immediately and the ALARM indicator to light. To resume normal on-line operations requires the operator to close the gate.

- PAPER fault (red light indicator under console cover)

When lit, this indicator warns that the paper is torn or that there is no paper. A PAPER fault causes the lineprinter to go off-line after printing the current line and the ALARM indicator to light. To resume normal on-line operations requires the operator to either load paper or advance the paper past the torn section.

- TAPE fault (red light indicator under console cover)

When lit, this indicator warns of a Vertical Forms Unit (VFU) error and causes the lineprinter go off-line after printing the current line and the ALARM indicator to light. To resume normal on-line operations requires the operator to either reload the VFU or replace the VFU tape.

Internal controls: Forms Reset switch, 6 LPI/8 LPI switch, Paper Width Adjustment, Phasing Control, Coarse and Fine Vertical Paper Adjustment, Horizontal Paper Adjustment, and Forms Thickness Adjustment.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Freestanding
Controller mounting code	One quad slot
Height	
LP11-A(B), LP11-E	43.8 in (111 cm)
LP11-C(D)	44.5 in (113 cm)
LP11-Y(Z)	45 in (114 cm)

## LINEPRINTERS

### Width

LP11-A(B), LP11-E	30.3 in (76 cm)
LP11-C(D)	33 in (84 cm)
LP11-Y(Z)	33 in (84 cm)

### Depth

LP11-A(B), LP11-E	33.6 in (85 cm)
LP11-C(D)	27.5 in (70 cm)
LP11-Y(Z)	26 in (66 cm)

### Weight

LP11-A(B), LP11-E	195 lbs (89 kg)
LP11-E	205 lbs (93 kg)
LP11-C(D)	435 lbs (197 kg)
LP11-Y(Z)	370 lbs (153 kg)

## PERFORMANCE

### Printing Speed

LP11-AA	300 l/min
LP11-BA	
64-character set	300 l/min
96-character set	215 l/min
LP11-EA	600 l/min
LP11-EB	
64-character set	600 l/min
96-character set	445 l/min
LP11-CA(CD)	900 l/min
LP11-DA(DD)	660 l/min
LP11-YA(YD)	600 l/min
LP11-ZA(ZD)	436 l/min

### Paper Slew Speed

LP11-A(B), LP11-E	15 in/sec (37.5 cm/sec)
LP11-C(D)	30 in/sec (76.2 cm/sec)
LP11-Y(Z)	25 in/sec (63.5 cm/sec)

## LINEPRINTERS

### ELECTRICAL

#### Starting (surge) current

LP11-AA, LP11-BA	6 A at 120 Vac 3 A at 240 Vac
LP11-EA	9 A at 120 Vac
LP11-EB	4.5 A at 240 Vac
LP11-CA, LP11-DA	15 A at 120 Vac
LP11-CD, LP11-DD	7.5 A at 240 Vac
Surge duration	2 s

#### Operating current

LP11-AA	3 A at 120 Vac
LP11-BA	1.5 A at 240 Vac
LP11-EA	4.5 A at 120 Vac
LP11-EB	2.25 A at 240 Vac
LP11-CA, LP11-DA	7 A at 120 Vac
LP11-CD, LP11-DD	3.5 A at 240 Vac
LP11-YA, LP11-ZA	4.5 A at 120 Vac
LP11-YD, LP11-ZD	2.25 A at 240 Vac
Interface (controller) current	1.5 A at +5Vdc

#### Power consumption

LP11-A(B)	350 Watts
LP11-E	475 Watts
LP11-C(D)	825 Watts
LP11-Y(Z)	680 Watts

#### Heat dissipation

LP11-A(B)	1200 Btus/hr
LP11-E	1619 Btus/hr

## LINEPRINTERS

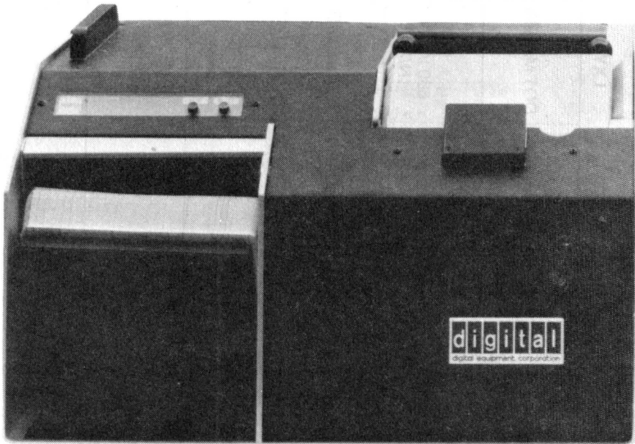
LP11-C(D)	2833 Btus/hr
LP11-Y(Z)	2319 Btus/hr
Operating voltage	120 Vac $\pm$ 10% 240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	
LP11-A(B), LP11-E	60 Hz $\pm$ 2 Hz 50 Hz $\pm$ 2 Hz
LP11-C(D), LP11-Y(Z)	60 Hz $\pm$ 1 Hz 50 Hz $\pm$ 1 Hz
Receptacles	Nema #5-15R, Nema #6-15R
Line cord length	12 ft

### ENVIRONMENTAL

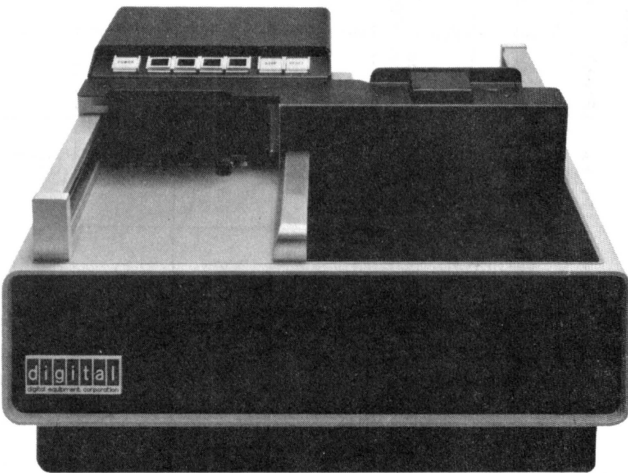
Operating temperature	50°F–104°F (10°C–40°C) 50°F–100°F (10°C–38°C)
Storage temperature	-40°F–150°F (-40°C–66°C) 0°F–150°F (-18°C–66°C)
Operating relative humidity	
LP11-A(B), LP11-E	20%–80% (non-condensing)
LP11-C(D)	10%–90% (non-condensing)
LP11-Y(Z)	30%–90% (non-condensing)
Storage relative humidity	
LP11-A(B), LP11-E, LP11-C(D)	10%–90% (non-condensing)
LP11-Y(Z)	5%–95% (non-condensing)
Maximum operating altitude	7,872 ft (2,400 m) above sea level

## LINE PRINTERS

	LP11-A	LP11-B	LP11-EA	LP11-EB	LP11-C	LP11-D	LP11-Y	LP11-Z	LXY11	LXY21
<b>TYPE</b>	BAND	BAND	BAND	BAND	DRUM	DRUM	DRUM	DRUM	DOT MATRIX	DOT MATRIX
<b>PRINTING SPEED</b> <b>96-CHAR. SET</b> <b>64-CHAR. SET</b>	N/A 300 l/min	215 l/min 300 l/min	N/A 600 l/min	445 l/min 600 l/min	N/A 900 l/min	660 l/min N/A	<sup>fi</sup> N/A 600 l/min	436 l/min N/A	300 l/min N/A	600 l/min N/A
<b>PVFU</b>	NONE	NONE	NONE	NONE	NONE	NONE	OPTIONAL	OPTIONAL	STANDARD	STANDARD
<b>OPTIONAL CHARACTER SETS</b>	YES	YES	YES	YES	NO	NO	NO	NO	YES	YES
<b>PLOT CAPABILITY</b>	NO	NO	NO	NO	NO	NO	NO	NO	YES	YES



**CR11(-A)**



**CR11-B**

## CHAPTER 5

# CARD READERS

### CR11 SERIES

The CR11(-A) and the CR11-BC(BD) are card reader systems mounted in self-contained tabletop units and connected to the UNIBUS via the controller. All CR11 card reader systems are supported by UNIBUS PDP-11 and VAX systems. The CR11(-A) versions were designed to operate at low speeds in light usage environments such as laboratory and industrial applications. The CR11-BC(BD) versions were designed to operate at medium speeds in medium usage environments such as engineering and industrial applications.

### FEATURES

- Reads hole punched cards only
- Two data formats selectable under program control: non-packed (standard Hollerith code) and packed (compressed Hollerith code)
- Long life expectancy and ease of maintenance
- Automatic shut-off feature
- Riffle air feature and short, straight card track for preventing card jams
- High reliability due to
  - six attempts to read a card before rejecting it
  - high tolerance to damaged cards
  - data resynchronization logic—allows punched holes to be read that are misaligned by 50% greater than the ANSI standard deviation (CR11-BC, CR11-BD versions only)

### DESCRIPTION

All versions of the CR11 card reader system consist of an input hopper for loading cards, a photoelectric read station for reading data from cards, an output stacker for stacking cards after reading, a motorized mechanism for moving the cards from the input hopper via the read station to the output stacker, a controller, a 25 ft (7.6 m) cable for connecting the card reader to the controller, and an internal clock for generating timing marks. The controller monitors the status of card reader operations, issues appropriate control commands, and handles data transfers between the card reader and the UNIBUS.

The card reader outputs visual signals (indicator lights) to indicate error conditions such as a torn card, a card with a damaged leading edge, cards stapled together, a card jam, and certain conditions such as "hopper empty/stacker full" and "unit busy".

The CR11 card reader systems process only standard 12-row, 80-column EIA (Hollerith code) hole punched cards. The CR11 and the CR11-A read up to 285 cards per minute and have an input hopper/output stacker capacity of 550 cards. The CR11-BC and the CR11-BD versions read up to 600 cards per minute and have an input hopper/output stacker capacity of 1000 cards.

Cards may be loaded and unloaded while the card reader is operating. Additional cards may be loaded provided the input hopper is approximately one-half to two-thirds empty.

### **OPERATION**

Before operation begins, the processor places an address on the UNIBUS, which the controller decodes to determine if the card reader is the selected external device. If so, the address selection logic then decodes the incoming address which is one of four possible sequential UNIBUS addresses. These four addresses correspond to the four controller registers, i.e., the Status Register, the Maintenance Register, and the two Data Buffer Registers (one for non-packed or 12-bit data and one for packed or 8-bit data). The register that is selected and the type of bus data transfer operation to be performed determine whether a command is to be issued, the status of the card reader is to be monitored, or data is to be read from a card in either of the two data formats.

Operation begins when the controller issues a READ command. The card reader is ready to accept a READ command when both the READER READY STATUS and BUSY bits in the controller status register are clear. The card reader is busy and cannot accept a READ command when the BUSY bit is set. The card reader is off-line when the READER READY STATUS bit is set.

When the card reader receives the READ command, it takes the first card from the hopper and feeds it into the motorized mechanism which moves the card into the read station. At the read station all 12 rows of all 80 columns of the card are read by a series of 12 photoelectric sensing devices column-by-column, beginning with column one. The card reader internal clock generates one timing mark for each card column read. After a column has been read, the 12 data bits, corresponding to the 12 rows of the card column, are placed into a 12-



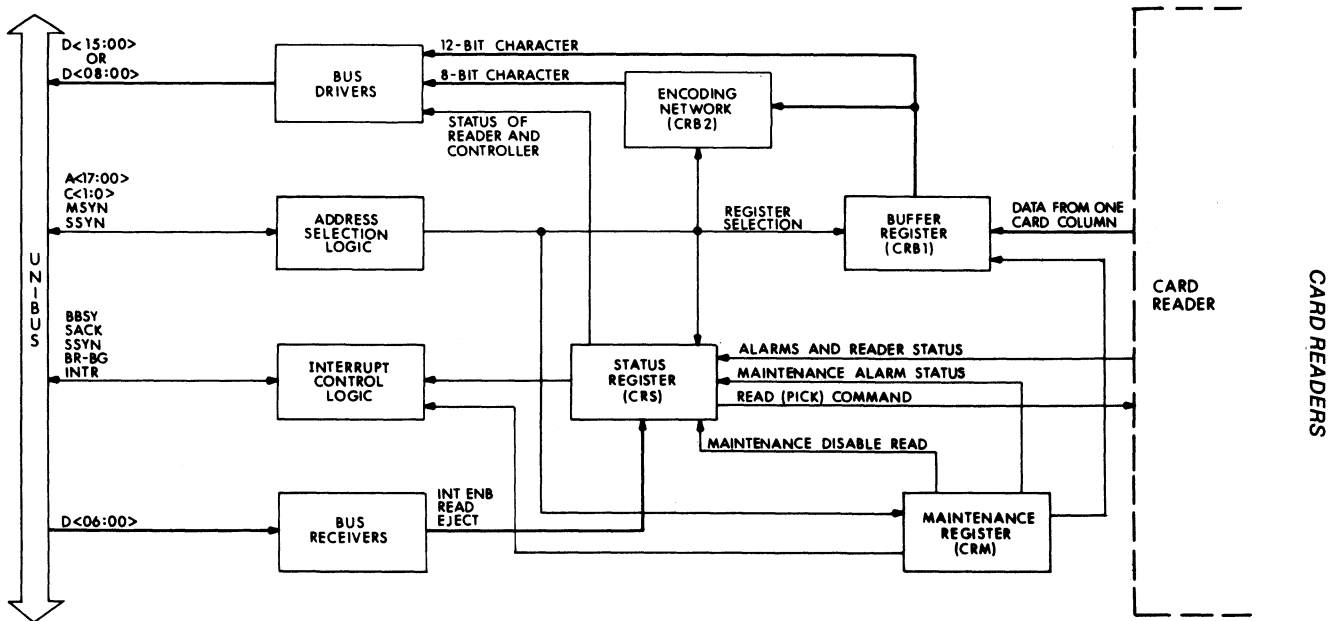


Figure 5-1 CR11 SYSTEM BLOCK DIAGRAM

bit register located inside the card reader and are gated in parallel, along with the timing mark, into the data buffer registers in the controller via the interconnect cable. Once the data buffer registers are loaded, the controller sets the COLUMN READY bit in the status register which generates an interrupt to alert the processor that the data is ready to be read. In response to the interrupt, the program will then read either of the two data buffer registers: CRB1 (12-bit non-packed data) or CRB2 (8-bit packed data). The COLUMN READY bit is cleared once the selected data buffer register has been read. If the program does not read one of the data buffer registers before the card reader reads another card column of data, the TIMING ERROR bit in the status register is set.

The status register can serve either as a command register to specify certain functions to be performed or as a status register to monitor operations within the controller and the card reader. When the status register functions as a command register, it is loaded from the UNIBUS and can perform one or more of the following functions: read, eject, or interrupt enable. The read (pick) function is the only command sent to the card reader and is used to start operation, i.e. causes the card reader to feed a card into the read station. The eject function causes the controller to skip the remainder of the card being read, although data is still transferred between the card reader and the data buffer registers. Interrupt enable allows an interrupt to be generated whenever 1) the reading of a card column or an entire card is completed 2) an error occurs 3) the card reader goes on-line or off-line.

When the status register is used to monitor system functions, it outputs status information to the UNIBUS for monitoring under program control. Some of the bits in the status register are set or cleared by error and status signals from the card reader itself, while others are set or cleared by error and status signals from the controller.

### **INTERRUPTS**

The CR11 system controller uses a bus request (BR) interrupt to gain control of the UNIBUS to perform a vectored interrupt, which causes the program to branch to an interrupt service routine. A BR interrupt can occur only if the INTERRUPT ENABLE bit in the status register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever any one of the following bits in the status register is set: ERROR, CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY.

When the ERROR bit is set, it indicates that some error condition exists and an interrupt is generated to cause the program to branch to an

error handling routine. When the CARD DONE, TRANSITION TO ONLINE, or COLUMN READY bits are set, the controller is ready to perform a data transfer or accept a command and an interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 6 and the interrupt vector address is 230. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### **DATA FORMATS**

Card data may be transferred to the UNIBUS in either of two formats, non-packed or packed. The non-packed data format is also referred to as normal while the packed format is known as compressed. In both modes, a punched hole is interpreted as a binary one and the absence of a hole as a binary zero.

In the non-packed, or normal, mode of operation, data is compatible with the standard EIA (Hollerith) code.‡ In this mode, data is read, placed in a 12-bit register located inside the card reader, and transferred in parallel to the controller data buffer register, CRB1. (Refer to the card reader register section in the back of this book for the CRB1 diagram.) Data is transferred directly from the 12 rows (zones) of the card to the corresponding bits <11-00> in the controller data buffer register (CRB1) for transfer to the UNIBUS.

The packed, or compressed data, mode of operation is compatible with the proposed expanded EIA (Hollerith) code. In this mode, data is transferred directly from the 5 rows, 8-12, of the card to the corresponding bits <07-03> in the controller data buffer register, CRB2, for transfer to the UNIBUS. (Refer to the card reader register section in the back of this book for the CRB2 diagram.) The encoded 3-bit octal representation of card rows 1-7 is loaded into bits <02-00>. This is possible because of the lack of double punches in rows 1-7 of Hollerith code. Since it compresses the 12 bits of data from the card column into an 8-bit character that is transferred to the UNIBUS as a low-order byte, the packed mode of operation results in more efficient data storage.

### **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy, minimal card jams and card wear, and continuous smooth processing of the card reader system.

‡ See Appendix A for standard and compressed Hollerith code chart.

Special design features of the CR11 card reader systems give them these qualities of high reliability as well as ease of maintenance.

- CR11 card reader system read stations use long-life infrared light-emitting diodes (LEDs) for their light source and 12 phototransistors for their sensors. The single piece construction of the read station makes adjustment easy.
- The shutdown switch on the rear panel may be set to provide continuous running (manual) or system power shut-off (automatic) after the last card has been read. The automatic shut-off feature reduces energy consumption and increases system life expectancy.
- CR11 card reader systems have a high tolerance to cards that have been nicked, warped, bent, or subjected to high humidity.
- Cards that have been stapled or taped together, unless such taping is on the leading edge (before the first data column), are not accepted.
- CR11 card reader systems vacuum picker automatically makes six attempts to process a card before rejecting it and generating a MOTION (PICK) CHECK error.
- A special riffle air feature at the input hopper of the all CR11 card reader systems (the CR11-BC and the CR11-BD versions have this feature at the output hopper as well) subjects the bottom half-inch of cards to a stream of air that separates the cards and air cushions them from the rest of the deck and from each other. This is important in preventing card jams since adjacent cards with a high concentration of punched holes tend to jam.
- The short, straight card path also minimizes card jams since only one card is in motion at any time.

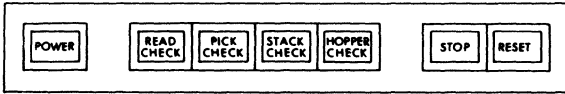
## **PANEL CONTROLS AND INDICATORS**

CR11 card reader systems can operate in either local or remote operating mode by setting the mode switch on the rear control panel to either remote (on-line) or local (off-line). Local mode is controlled by pushbuttons on the front control panel while remote mode operates under program control. The front panel controls and indicators are used for normal on-line/off-line operations while the rear panel indicators are used for initial system set-up and maintenance. The indicator lights provide card reader status information.

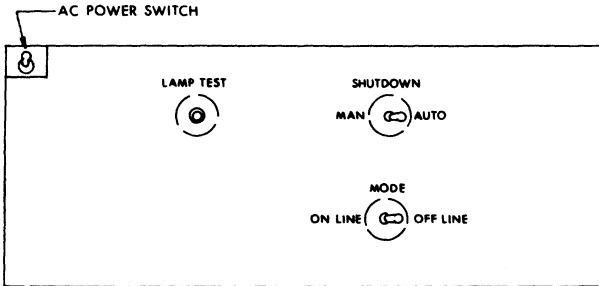
- **POWER** switch for CR11, CR11-A versions (2-position toggle switch on rear panel and associated white light indicator on front panel)

Controls application of all power to the card reader. When the toggle switch is set to on, it applies power to the card reader and causes the associated indicator to light. When the toggle switch is set to off,

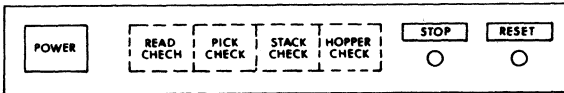
CARD READERS



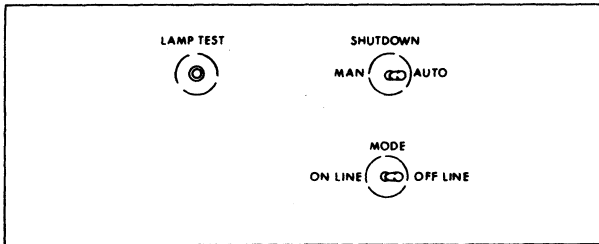
CR11, CR11-A FRONT PANEL



CR11, CR11-A REAR PANEL



CR11-BC, CR11-BD FRONT PANEL



CR11-BC, CR11-BD REAR PANEL

Figure 5-2 CR11 CONTROLS AND INDICATORS

it removes all power from the card reader and causes the associated indicator to go out.

- **POWER** switch for CR11-BC, CR11-BD versions (alternate-action pushbutton/white light indicator on front panel)

This switch controls application of all power to the card reader. When depressed, power is applied to the card reader and the indicator lights. When depressed again, power is removed from the card reader and the indicator light goes out.

- **READ CHECK** lamp (white light indicator on front panel)

When lit, this indicator warns that the card just read may be torn on the leading or trailing edges, or that the card may have punches in the 0 or 81st columns. When the READ CHECK indicator is lit, denoting an error condition, the card reader stops operation and the RESET indicator goes out.

- **PICK CHECK** lamp (white light indicator on front panel)

When lit, this indicator signals the failure of the card reader to move a card into the read station after it received a READ command from the controller. When the PICK CHECK indicator is lit, denoting an error condition, the card reader stops operation and the RESET indicator goes out.

- **STACK CHECK** lamp (white light indicator on front panel)

When lit, this indicator signals improper seating and possible damage to the previous card in the output stacker. When the STACK CHECK indicator is lit, denoting an error condition, the card reader stops operation and the RESET indicator goes out.

- **HOPPER CHECK** lamp (white light indicator on front panel)

When lit, this indicator warns that either the input hopper is empty or that the output stacker is full. When the HOPPER CHECK indicator is lit, denoting an error condition, the card reader stops operation and the RESET indicator goes out. The operator must manually correct the condition before card reader operation can continue.

- **STOP** switch (momentary pushbutton/red light indicator on front panel)

When depressed, this indicator immediately lights, the RESET indicator light goes out, and the READER READY STATUS bit in the controller status register is set indicating that the card reader is off-line. Card reader operation stops as soon as the card currently in the read station has been read. This switch has no effect on system power, it merely stops the current operation.

## CARD READERS

- **RESET switch** (momentary pushbutton/green light indicator on front panel)

When depressed, this indicator clears all error flip-flops and initializes all counters. When depressed, the RESET indicator light comes on and the READER READY STATUS bit in the controller status register is cleared indicating that the card reader is on-line. The RESET indicator light goes out whenever the STOP indicator light or an error indicator light (READ CHECK, PICK CHECK, STACK CHECK, or HOPPER CHECK) comes on.

- **LAMP TEST switch** (momentary pushbutton on rear panel)

When depressed, this switch causes all the indicators on the front control panel to light to determine if any of the indicator lamps are faulty.

- **SHUTDOWN switch** (2-position toggle switch on rear panel)

This switch controls automatic operation of the input hopper blower. When set to MANUAL, the blower and drive motors operate continuously whether or not cards are in the input hopper. When set to AUTOMATIC, the blower and drive motors shut off automatically whenever the input hopper is empty. The drive motors will automatically restart when cards are loaded into the input hopper and the RESET switch is depressed.

- **MODE switch** (2-position toggle switch on rear panel)

This switch permits selection of either remote (on-line) or local (off-line) operation of the card reader system. When set to LOCAL, the operator controls the card reader off-line by using the RESET and STOP switches on the front control panel. When set to REMOTE, normal on-line operation under program control resumes once the RESET switch has been depressed.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Tabletop
Controller mounting code	One quad slot
Height	
CR11(-A)	11 in (27.9 cm)
CR11-BC(BD)	16.25 in (41.3 cm)
Width	
CR11(-A)	19.25 in (48.9 cm)
CR11-BC(BD)	23 in (58.4 cm)

## CARD READERS

### Depth

CR11(-A) 14 in (35.6 cm)

CR11-BC(BD) 18 in (45.7 cm)

### Weight

CR11(-A) 60 lbs (27.2 kg)

CR11-BC(BD) 75 lbs (34 kg)

## PERFORMANCE

### Card rate

CR11(-A) 285 cards per minute

CR11-BC(BD) 600 cards per minute

### Input hopper/Output stacker capacity

CR11(-A) 550 cards

CR11-BC(BD) 1000 cards

## ELECTRICAL

### Starting (surge) current

CR11 18 A at 120 Vac

CR11-A 9 A at 240 Vac

CR11-BC 12 A at 120 Vac

CR11-BD 6 A at 240 Vac

### Surge duration

CR11, CR11-A 3 s

CR11-BC, CR11-BD 6 s

### Operating current

CR11 5 A at 120 Vac

CR11-A 2.5 A at 240 Vac

CR11-BC 6 A at 120 Vac

CR11-BD 3 A at 240 Vac

Interface (controller) current 1.5 A at +5 Vdc

### Power consumption

CR11, CR11-A 600 Watts

CR11-BC, CR11-BD 700 Watts

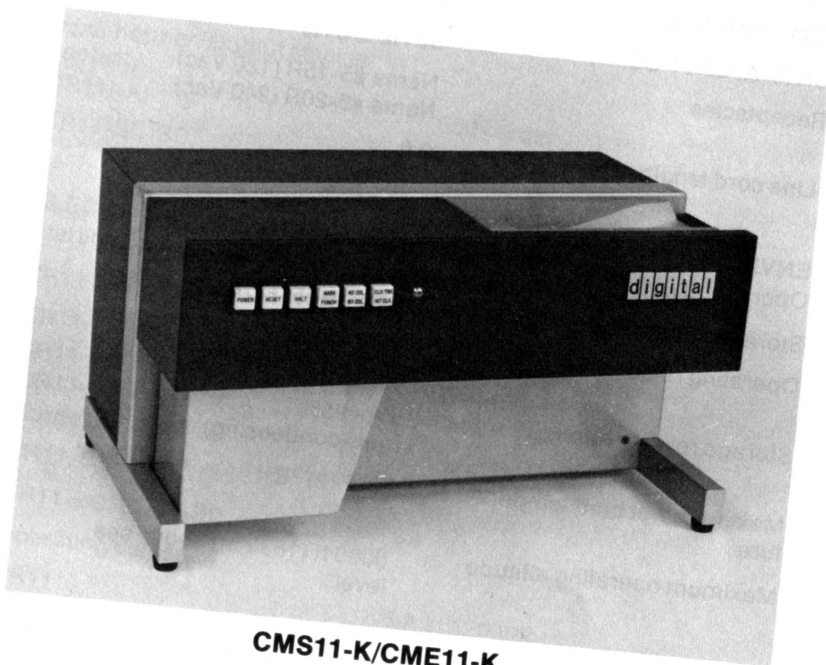


## CARD READERS

Heat dissipation	
CR11, CR11-A	2046 Btus/hr
CR11-BC, CR11-BD	2387 Btus/hr
Operating voltage	
CR11, CR11-BC	120 Vac $\pm$ 10%
CR11-A, CR11-BD	240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	
CR11, CR11-BC	60 Hz $\pm$ 3 Hz
CR11-A, CR11-BD	50 Hz $\pm$ 3 Hz
Receptacles	Nema #5-15R (120 Vac), Nema #6-20R (240 Vac)
Line cord length	9 ft

### **ENVIRONMENTAL**

Operating temperature	50°F–100°F (10°C–38°C)
Storage temperature	-25°F–135°F (-46°C–43°C)
Operating relative humidity	30%–90% (non-condensing)
Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	80°F (27°C)
Maximum operating altitude	6000 ft (1830 m) above sea level



**CMS11-K/CME11-K**

**CMS11/CME11**

The CMS11-KA(KB) and the CME11-KA(KB) are DIGITAL's lowest priced card reader systems. They are mounted in self-contained tabletop units and connected to the UNIBUS via the controller. The CMS11-K versions are supported by UNIBUS PDP-11 systems while the CME11-K versions are supported by VAX systems. All versions were designed to operate at low speeds in light usage environments such as educational and telephone industry applications.

**FEATURES**

- Reads hole punched and mark sense cards
- Two data formats selectable under program control: non-packed (standard Hollerith code) and packed (compressed Hollerith code)
- Long life expectancy and ease of maintenance
- Short, straight card track for preventing card jams
- High reliability due to
  - three attempts to read a card before rejecting it
  - high tolerance to damaged cards
  - data resynchronization logic—allows punched holes to be read that are misaligned by 50% greater than the ANSI standard deviation

**DESCRIPTION**

All versions of the CMS11-K/CME11-K card reader system consist of an input hopper for loading cards, a photoelectric read station for reading data from cards, an output stacker for stacking cards after reading, a motorized mechanism for moving the cards from the input hopper via the read station to the output stacker, a controller, a 25 ft (7.6 m) cable for connecting the card reader to the controller, and an internal clock for generating timing marks. The controller monitors the status of card reader operations, issues appropriate control commands, and handles data transfers between the card reader and the UNIBUS.

The CMS11-K and the CME11-K card reader systems process standard 12-row, 80-column EIA (Hollerith) code hole punched cards with or without timing marks as well as 12-row, 40- or 80-column mark sense cards with or without timing marks. The card reader systems are also capable of reading marks and punched holes intermixed on

the same card as long as mark sense cards are used. The CMS11-KA and the CME11-KA read up to 250 cards per minute while the CMS11-KB and the CME11-KB read up to 200 cards per minute. All versions have an input hopper/output stacker capacity of 250 cards.

Cards may be loaded and unloaded while the card reader is operating. Additional cards may be loaded provided the input hopper is approximately one-half to two-thirds empty.

## **OPERATION**

Before operation begins, the processor places an address on the UNIBUS, which the controller decodes to determine if the card reader is the selected external device. If so, the address selection logic then decodes the incoming address which is one of four possible sequential UNIBUS addresses. These four addresses correspond to the four controller registers, i.e., the Status Register, the Maintenance Register, and the two Data Buffer Registers (one for non-packed or 12-bit data and one for packed or 8-bit data). The register that is selected and the type of bus data transfer operation to be performed determine whether a command is to be issued, the status of the card reader is to be monitored, or data is to be read from a card in either of the two data formats.

Operation begins when the controller issues a READ command. The card reader is ready to accept a READ command when both the READER READY STATUS and BUSY bits in the controller status register are clear. The card reader is busy and cannot accept a READ command when the BUSY bit is set. The card reader is off-line when the READER READY STATUS bit is set.

When the card reader receives the READ command, it takes the first card from the hopper and feeds it into the motorized mechanism which moves the card into the read station. At the read station all 12 rows of all 80 columns of the card are read by a series of 12 photoelectric sensing devices column-by-column, beginning with column one. The card reader internal clock generates one timing mark for each card column read. After a column has been read, the 12 data bits, corresponding to the 12 rows of the card column, are placed into a 12-bit register located inside the card reader and are gated in parallel, along with the timing mark, into the data buffer registers in the controller via the interconnect cable. Once the data buffer registers are loaded, the controller sets the COLUMN READY bit in the status register which generates an interrupt to alert the processor that the data is ready to be read. In response to the interrupt, the program will then read either of the two data buffer registers: CRB1 (12-bit non-packed data) or CRB2 (8-bit packed data). The COLUMN READY bit is cleared

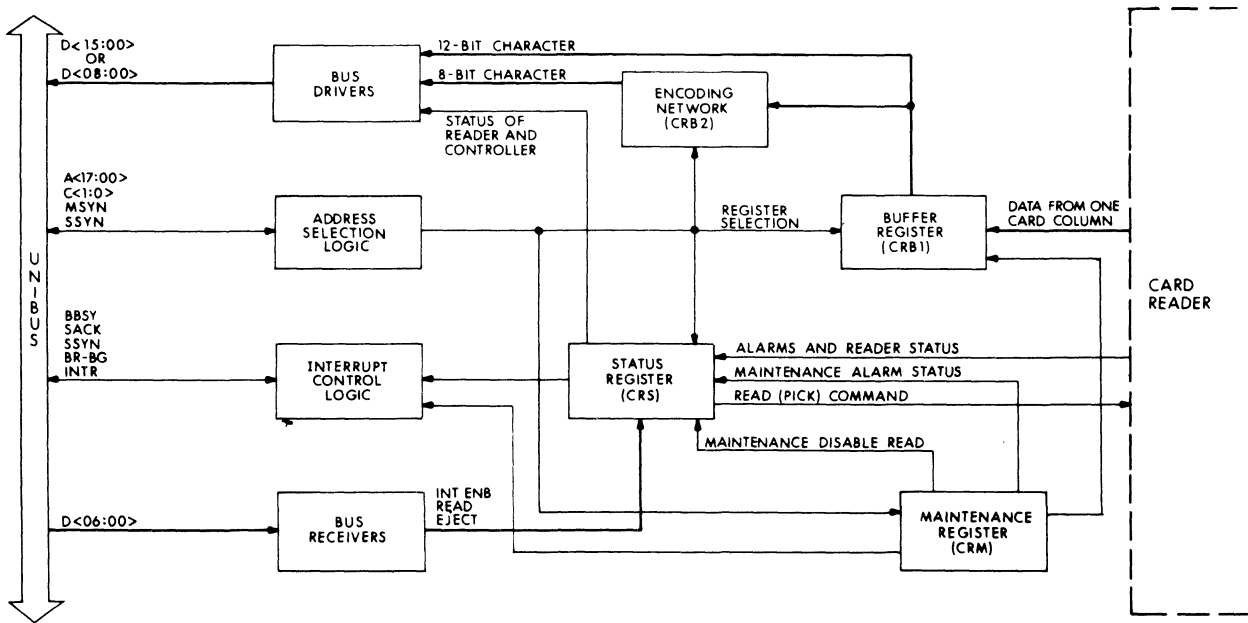


Figure 5-3 CMS11/CME11 SYSTEM BLOCK DIAGRAM

once the selected data buffer register has been read. If the program does not read one of the data buffer registers before the card reader reads another card column of data, the TIMING ERROR bit in the status register is set.

The status register can serve either as a command register to specify certain functions to be performed or as a status register to monitor operations within the controller and the card reader. When the status register functions as a command register, it is loaded from the UNIBUS and can perform one or more of the following functions: read, eject, or interrupt enable. The read (pick) function is the only command sent to the card reader and is used to start operation, i.e. causes the card reader to feed a card into the read station. The eject function causes the controller to skip the remainder of the card being read, although data is still transferred between the card reader and the data buffer registers. Interrupt enable allows an interrupt to be generated whenever 1) the reading of a card column or an entire card is completed 2) an error occurs 3) the card reader goes on-line or off-line.

When the status register is used to monitor system functions, it outputs status information to the UNIBUS for monitoring under program control. Some of the bits in the status register are set or cleared by error and status signals from the card reader itself, while others are set or cleared by error and status signals from the controller.

## **INTERRUPTS**

The CMS11-K/CME11-K system controller uses a bus request (BR) interrupt to gain control of the UNIBUS to perform a vectored interrupt, which causes the program to branch to an interrupt service routine. A BR interrupt can occur only if the INTERRUPT ENABLE bit in the status register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever any one of the following bits in the status register is set: ERROR, CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY.

When the ERROR bit is set, it indicates that some error condition exists and an interrupt is generated to cause the program to branch to an error handling routine. When the CARD DONE, TRANSITION TO ON-LINE, or COLUMN READY bits are set, the controller is ready to perform a data transfer or accept a command and an interrupt request is made so that the program can branch to an interrupt service routine.

The interrupt priority level is 6 and the interrupt vector address is 230. Note that the priority level can be changed with a priority plug and the

vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### **DATA FORMATS**

Card data may be transferred to the UNIBUS in either of two formats, non-packed or packed. The non-packed data format is also referred to as normal while the packed format is known as compressed. In both modes, a punched hole is interpreted as a binary one and the absence of a hole as a binary zero.

In the non-packed, or normal, mode of operation, data is compatible with the standard EIA (Hollerith) code.‡ In this mode, data is read, placed in a 12-bit register located inside the card reader, and transferred in parallel to the controller data buffer register, CRB1. (Refer to the card reader register section in the back of this book for the CRB1 diagram.) Data is transferred directly from the 12 rows (zones) of the card to the corresponding bits <11-00> in the controller data buffer register (CRB1) for transfer to the UNIBUS.

The packed, or compressed data, mode of operation is compatible with the proposed expanded EIA (Hollerith) code. In this mode, data is transferred directly from the 5 rows, 8-12, of the card to the corresponding bits <07-03> in the controller data buffer register, CRB2, for transfer to the UNIBUS. (Refer to the card reader register section in the back of this book for the CRB2 diagram.) The encoded 3-bit octal representation of card rows 1-7 is loaded into bits <02-00>. This is possible because of the lack of double punches in rows 1-7 of Hollerith code. Since it compresses the 12 bits of data from the card column into an 8-bit character that is transferred to the UNIBUS as a low-order byte, the packed mode of operation results in more efficient data storage.

### **RELIABILITY/MAINTAINABILITY**

Reliability means long life expectancy, minimal card jams and card wear, and continuous smooth processing of the card reader system. Special design features of the CMS11-K and the CME11-K card reader systems give them these qualities of high reliability as well as ease of maintenance.

- CMS11-K and CME11-K card reader system read stations use long-life infrared light-emitting diodes (LEDs) for their light source and 12 phototransistors for their sensors.

‡ See Appendix A for standard and compressed Hollerith code chart.

- CMS11-K and CME11-K card reader systems have a high tolerance to cards that have been nicked, warped, bent, or subjected to high humidity.
- Cards that have been stapled or taped together, unless such taping is on the leading edge (before the first data column), are not accepted.
- CMS11-K and CME11-K card reader system friction pickers automatically make three attempts to process a card before rejecting it and generating a MOTION CHECK error.
- The short, straight card path also minimizes card jams since only one card is in motion at any time.

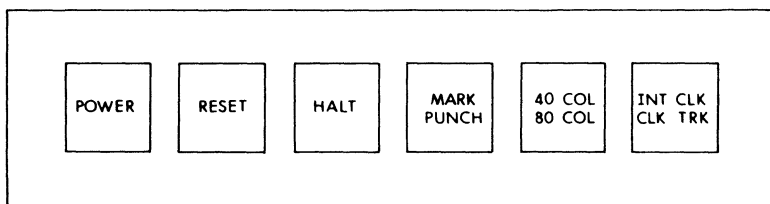


Figure 5-4 CMS11/CME11 FRONT PANEL CONTROLS

### PANEL CONTROLS AND INDICATORS

The front panel controls allow the operator to control the card reader manually. The indicator lights provide card reader status information.

- **POWER** switch (alternate-action pushbutton/white light indicator switch on front panel)

This switch controls application of all power to the card reader. When depressed, power is applied to the card reader and the indicator lights up. When depressed again, power is removed from the card reader and the indicator light goes out.

- **RESET** switch (momentary pushbutton/white light indicator on front panel)

When lit, this switch indicates that the card reader has gone off-line, i.e. that the **READER READY STATUS** bit in the controller status register has been set, due to either an error condition (**HOPPER CHECK**, **MOTION CHECK**) or the **HALT** switch having been depressed. To resume normal on-line operation requires operator intervention. Depressing the switch causes the indicator light to go out and the **READER READY STATUS** bit in the controller status register to be cleared indicating that the card reader is on-line, providing that the error condition has been corrected.



- **HALT switch** (momentary pushbutton on front panel)

When depressed, this switch causes the RESET indicator to light, which in turn causes the READER READY STATUS bit in the controller status register to be set, shutting down operation of the card reader drive motor and putting the card reader off-line to the controller.

- **MARK/PUNCH switch** (alternate-action pushbutton/white light split indicator on front panel)

When the MARK half of the split indicator is lit, the card reader is conditioned to read mark sense cards. Mark sense cards may use marks only or may intermix marks and punched holes on the same card. When the PUNCH half of the split indicator is lit, the card reader is conditioned to read hole punched cards only.

- **40/80 COLUMN switch** (alternate-action pushbutton/white light split indicator on front panel)

When the 40 half of the split indicator is lit, the card reader is conditioned to read 40 column cards only. When the 80 half of the split indicator is lit, the card reader is conditioned to read 80 column cards only. When the INTERNAL CLOCK/CLOCK TRACK (INT CLK/CLK TRK) switch is set to CLOCK TRACK (CLK TRK), the 40/80 COLUMN switch is set to 80.

- **INTERNAL CLOCK/CLOCK TRACK (INT CLK/CLK TRK, alternate-action pushbutton/white light split indicator on front panel)**

When the INTERNAL CLOCK (INT CLK) half of the split indicator is lit, the card reader is conditioned to use internal or device timing. When the CLOCK TRACK (CLK TRK) half of the split indicator is lit, the card reader is conditioned to read the timing marks printed in the clock tracks of the cards.

## SPECIFICATIONS

### MECHANICAL

Cabinet	Tabletop
Controller mounting code	One quad slot
Height	10.75 in (27.3 cm)
Width	19.25 in (48.9 cm)
Depth	11.75 in (29.8 cm)
Weight	32 lbs (14.5 kg)

## CARD READERS

### PERFORMANCE

Card rate	250 cards per minute
Input hopper/Output stacker capacity	200 cards

### ELECTRICAL

Starting (surge) current	
CMS11-KA, CME11-KA	6 A at 120 Vac
CMS11-KB, CME11-KB	6 A at 240 Vac
Surge duration	5 s
Operating current	
CMS11-KA, CME11-KA	1 A at 120 Vac
CMS11-KB, CME11-KB	.9 A at 240 Vac
Interface (controller) current	1.5 A at +5 Vdc
Power consumption	185 Watts
Heat dissipation	630 Btus/hr
Operating voltage	
CMS11-KA, CME11-KA	120 Vac $\pm$ 10%
CMS11-KB, CME11-KB	240 Vac $\pm$ 10%
Phase	1-Phase
Line frequency	
CMS11-KA, CME11-KA	60 Hz $\pm$ 3 Hz
CMS11-KB, CME11-KB	50 Hz $\pm$ 3 Hz
Receptacles	Nema #5-15R (120 Vac), Nema #6-20R (240 Vac)
Line cord length	8 ft

### ENVIRONMENTAL

Operating temperature	50°F–95°F (10°C–35°C)
Storage temperature	-40°F–140°F (-40°C–60°C)
Operating relative humidity	20%–80% (non-condensing)

## *CARD READERS*

Storage relative humidity	5%–95% (non-condensing)
Maximum wet bulb temperature	89°F (32°C)
Maximum operating altitude	10,000 ft (3050 m) above sea level

**CARD READERS**

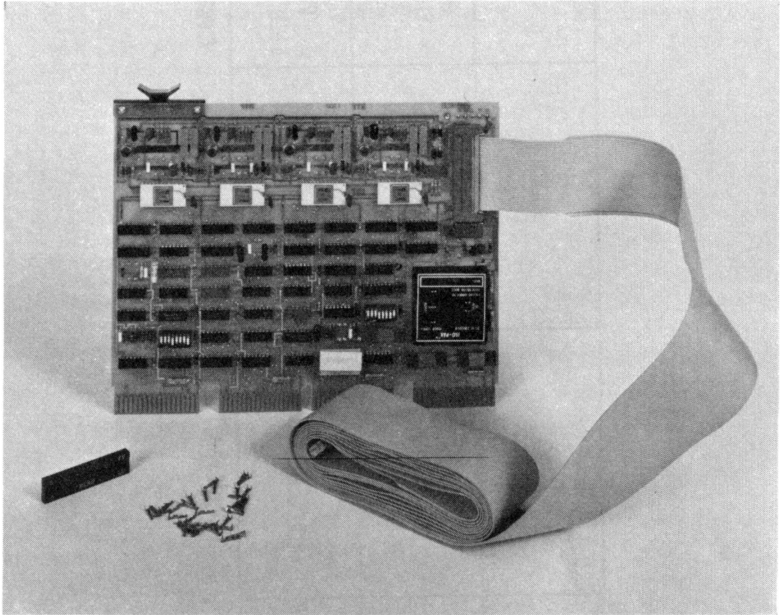
**CR11(-A)**

**CR11-B**

**CMS11-K/CME11-K**

<b>CARD TYPE</b>	HOLE PUNCHED	HOLE PUNCHED	HOLE PUNCHED OR MARK SENSE
<b>CARD RATE</b>	285	600	250
<b>INPUT HOPPER/ OUTPUT STACKER CAPACITY</b>	550	1000	200





**AA11-K**

## CHAPTER 6

# SENSOR I/O DEVICES

### AA11-K

The AA11-K is a four-channel independently buffered, 12-bit, digital-to-analog converter (DAC) and associated display control. It is supported by UNIBUS PDP-11 systems on the UNIBUS or on the LPA11-K bus with a KW11-K programmable realtime clock and by VAX-11 systems only on the LPA11-K bus with a KW11-K. The AA11-K is used in applications such as acoustics, process control, and flight simulation.

### FEATURES

- Four independently buffered digital-to-analog channels
- Jumper-selectable output ranges of -5 Vdc to +5 Vdc, -10 Vdc to +10 Vdc, and -0.5 Vdc to +0.5 Vdc

### DESCRIPTION

Under program control, the AA11-K provides analog outputs and digital control signals to operate oscilloscopes (Tektronix 602, 604 display oscilloscopes and 611, 613 storage oscilloscopes) and other CRTs, X/Y recorders, and strip chart recorders.

The AA11-K allows the user to output data in the form of a 4096 x 4096 dot array on an oscilloscope screen. Thus, a dot may be produced at any point in the array and a series of dots, programmed sequentially, produce graphic patterns.

Point plotting on oscilloscopes and other CRTs is done by converting the programmed information to analog voltages which are sent to X and Y inputs, which in turn set the beam at the desired dot position. After a brief delay, a digital INTENSIFY pulse is automatically sent. This causes the dot position where the beam is currently located to remain lit (stored), even after the beam has been repositioned.

Point-to-point plotting on a X/Y recorder is also done by transforming the programmed information into voltages which are sent to X and Y inputs, which in turn position the pen on the paper instead of setting the beam of an oscilloscope. A digital signal lowers the pen and another set of voltages input to X and Y will cause the pen to draw a straight line along the paper to the new position. Repeated operations will result in graphic patterns. The programmed information consists of a continuous stream of numbers, converted to a continuous stream of voltages, which generate a sequence of pen operations. Because the operations are not necessarily sequential, that is the pen can be lifted to an non-adjacent point between lines, lines drawn on the paper

can be from any point or just a point can be drawn.

Plotting on a strip chart recorder is also done by transforming the programmed information into voltages which are sent to the recorder, and these position the pen or pens on the paper. A strip chart recorder may use up to four pens, one pen for each channel. As the paper strip moves along, each pen moves across the width of the paper to the position specified by the voltage. The programmed information consists of a continuous stream of numbers, converted to a continuously varying voltage, which causes the pen or pens to produce graphic output.

### **OPERATION**

The AA11-K has five registers: the Display Status Register and four Data Buffer Registers. (Refer to the register section at the back of this book for register diagrams and bit definitions). The four 12-bit data buffer registers correspond to the four 12-bit digital-to-analog converters (DACs).

Output operations are accomplished by loading the four digital-to-analog data buffer registers and the display status register. When the AA11-K is connected to an oscilloscope, two of the data buffer registers are loaded with the desired coordinates of the dot position. After the proper delay, the AA11-K automatically generates an INTENSIFY pulse. The other two data buffer registers are not used for controlling oscilloscopes. By loading bits in the display status register, the user's program can store a graphic pattern on the oscilloscope screen, erase the screen, or superimpose a moveable pattern on a previously stored pattern.

### **INTERRUPTS**

The AA11-K uses a bus request (BR) interrupt to gain control of the UNIBUS to perform a vectored interrupt, which causes the program to branch to an interrupt service routine. A BR interrupt can occur only if the INTERRUPT ENABLE bit in the Display Status Register is set. Once the INTERRUPT ENABLE bit is set, an interrupt request is generated whenever the READY bit in the Display Status Register is also set.

A BR interrupt is generated whenever a set of coordinates and the subsequent INTENSIFY pulse are sent to the oscilloscope and also at the completion of an erase operation.

The interrupt priority level is 4 and the interrupt vector address is 360. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.



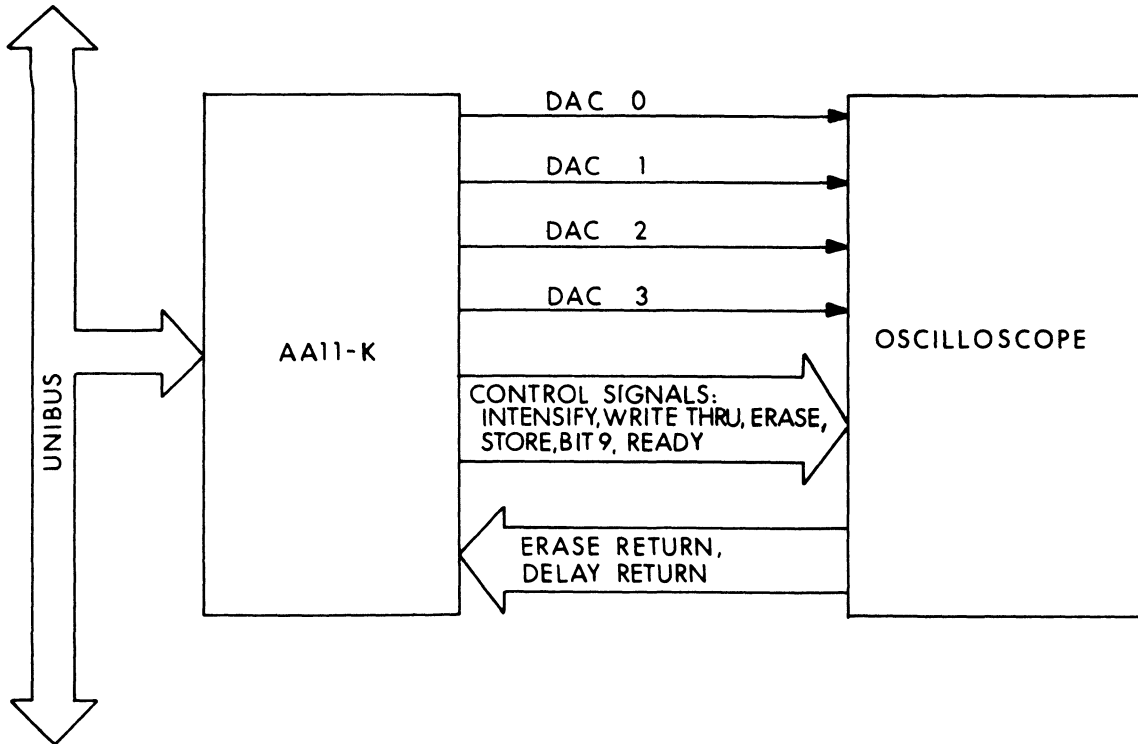


Figure 6-1 AA11-K BLOCK DIAGRAM



## SENSOR I/O DEVICES

### Logic outputs

NON-STORE L, WRITE THRU L, ERASE L, READY L      TTL open collector

BIT 9 L      TTL open collector, 1K pullup to +5 Vdc

### Logic inputs

ERASE RETURN L      Compatible with Tektronix 611, 613

DELAY RET L      TTL input

### **ELECTRICAL**

Current drawn      2.5 amps at +5 Vdc

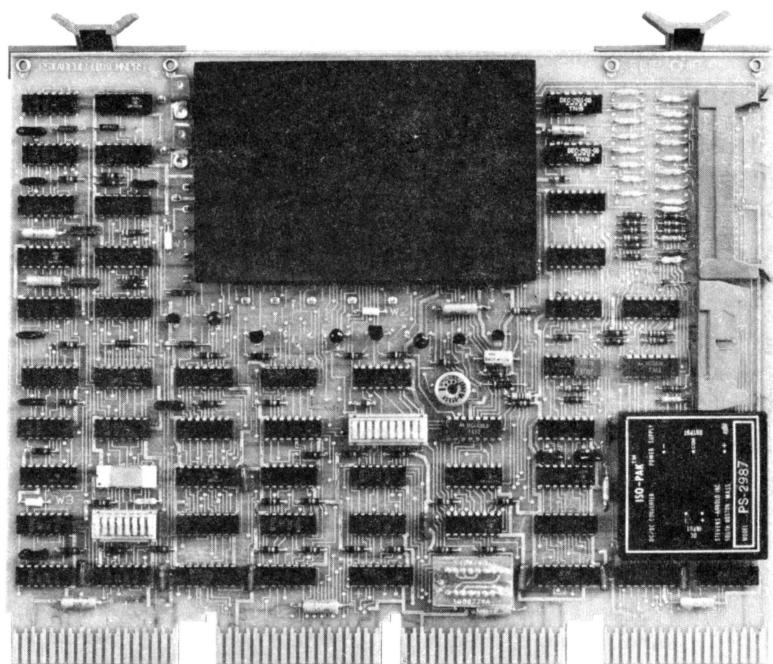
Warmup time      5 minutes minimum

### **ENVIRONMENTAL**

The AA11-K conforms to the individual system's environmental specifications.

Operating temperature      50°F–104°F (10°C–40°C)

Operating relative humidity      10%–90%  
(non-condensing)



AD11-K

**AD11-K**

The AD11-K is a double-buffered, 12-bit analog-to-digital converter with an input multiplexer that accepts up to 16 inputs. When used in conjunction with the AM11-K, the AD11-K accepts up to 64 inputs. The AD11-K is supported by UNIBUS PDP-11 systems on the UNIBUS or on the LPA11-K bus with a KW11-K programmable realtime clock and by VAX-11 systems only on the LPA11-K bus with a KW11-K. The AD11-K can be used in most applications involving data acquisition.

**FEATURES**

- Switch-selectable between 8 differential input channels or 16 single-ended input channels
- Jumper-selectable input ranges of -5 Vdc to +5 Vdc, -5.12 Vdc to +5.12 Vdc, -10 Vdc to +10 Vdc, -10.24 Vdc to +10.24 Vdc, 0 Vdc to +10 Vdc, and 0 Vdc to +10.24 Vdc
- Input over-voltage protection

**DESCRIPTION**

The AD11-K accepts analog input from up to sixteen laboratory options which it converts to a 12-bit digital numerical value. The AD11-K is switch-selectable between 8 differential input channels or 16 single-ended input channels. Although the channels are selected by the program, only one can be converted at a time. Analog-to-digital conversions can be initiated in any one of three ways: under program control, from a realtime clock (KW11-K), or from an external event.

**OPERATION**

The AD11-K has two registers: the Status Register and the Analog-to-Digital (A/D)/Digital-to-Analog (DAC) Buffer Register. The DAC Buffer Register is write-only and is loaded with data used to test the A/D converter. When this register is read, it contains the digital value of the analog input from the selected channel. The register is then referred to as the A/D Buffer Register. (Refer to the register section at the back of this book for register diagrams and bit definitions).

Input operations are accomplished by loading the status register and reading the A/D buffer register. The input channel is selected by loading bits in the status register. After selecting a channel, there is a delay of 10  $\mu$ s before the A/D converter starts the conversion process. Setting A/D START <00> will start a conversion immediately. Setting OVERFLOW ENABLE <05> permits overflow from a KW11-K realtime clock to initiate conversions. Setting EXTERNAL START ENABLE <04> permits an external input to initiate conversions. An A/D conversion takes approximately 12  $\mu$ s. When the conversion is completed, DONE <07> is set and an interrupt is generated. The converted value

is then read out of the A/D buffer register. Since the converted value is held in this buffer register, a second conversion can be initiated before the results of the first conversion are read, achieving a high throughput rate.

The 8-bit DAC converter, loaded by the DAC buffer register, allows analog data to be generated under program control to test the A/D converter. Since the DAC converter has no control logic, the software must provide approximately 30  $\mu$ s of delay before reading back the contents of the A/D buffer register.

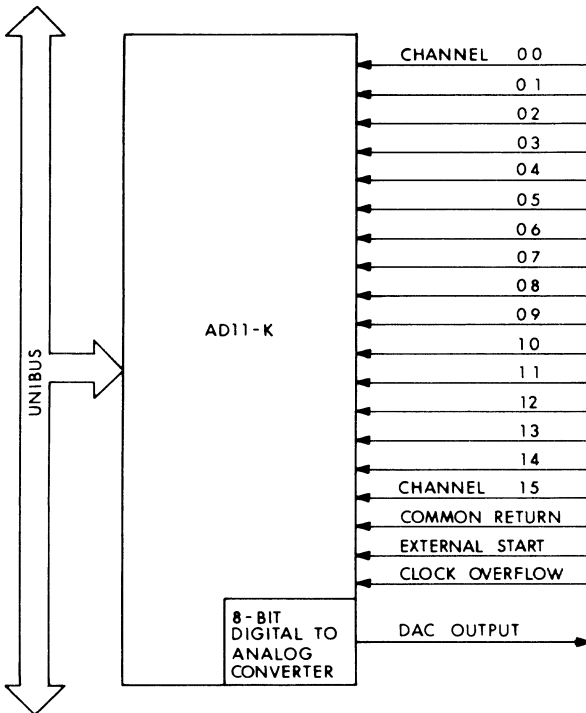


Figure 6-2 AD11-K BLOCK DIAGRAM



## SENSOR I/O DEVICES

Input slewing speed	7 Vdc/ $\mu$ s maximum
Interchannel settling error	$\pm 1$ Least Significant Bit maximum
Crosstalk	80 dB down at 1 kHz (15 unselected channels into one selected channel)
Differential common mode rejection	70 dB (dc to 1 kHz)
Throughput time	22 $\mu$ s (10 $\mu$ s to interchannel settling plus 12 $\mu$ s for A/D conversion)
Sample-and-hold aperture	200 $\pm$ 20 ns after external start 165 $\pm$ 20 ns after clock overflow 20 ns maximum, delay uncertainty

### ELECTRICAL

Current Drawn	3.5 amps at +5 Vdc
Warmup time	5 minutes minimum

### ENVIRONMENTAL

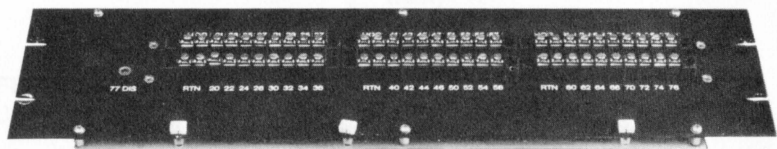
The AD11-K conforms to the individual system's environmental specifications.

Operating temperature	50°F–104°F (10°C–40°C)
Operating relative humidity	10%–90% (non-condensing)





Input/Output Speed	7 Voids per Hour
Input Channel Width	1/2 Inch Standard (31.75 mm)
Channels	40 Channels of 1 kHz 13 unselected channels into one selected channel
Display, when in non-modulation	70 dB to 1 kHz
Frequency Error	±2 µHz to 10 kHz ±10 µHz to 100 kHz ±100 µHz to 1 MHz
Stop-Band Attenuation	70 dB at 20 Hz after every 10 kHz 10 µHz at 10 kHz 20 Hz maximum error per channel



**AM11-K**

## AM11-K

The AM11-K is a multiplexer expander for use in conjunction with the AD11-K analog-to-digital converter to allow it to accept up to 64 inputs.

## FEATURES

- Jumper-selectable between 24 differential input channels or 48 single-ended input channels
- Switch-selectable input channel gain of 1, 4, 5, 16, 50, or 64
- Input over-voltage protection

## DESCRIPTION

The AM11-K is a multiplexer expander that, when used in conjunction with the AD11-K, allows the AD11-K to accept input from 64 laboratory options instead of the usual 16. The AM11-K includes a cable for connection to the AD11-K. The AM11-K input channels are divided into three groups. Each group is jumper-selectable between 8 differential input channels or 16 single-ended input channels. The analog input gain of each group is switch-selectable between 1, 4, 5, 16, 50, or 64. The gain of AD11-K input channels is always 1.

The processor communicates via the UNIBUS with the AD11-K only. When channels 20-77 are called for, the AD11-K will activate that channel in the AM11-K.

The hardware throughput rate for channels 20-77 in the AM11-K is 25 kHz, versus a 40 kHz rate for the AD11-K, because longer settling time is allotted to the gain amplifier in the AM11-K.

The AM11-K uses the built-in self-test circuitry in the AD11-K.

## PROGRAMMING

All communication to the AM11-K is handled by the AD11-K. An input channel in the AM11-K is selected by loading the proper bits into the AD11-K status register. The AD11-K, in turn, activates the desired channel in the AM11-K. After selecting a channel, there is a delay of 30  $\mu$ s before the A/D converter in the AD11-K starts the conversion process. A 10  $\mu$ s delay allows the input multiplexer time to settle, while an additional 20  $\mu$ s of delay allows the gain amplifier time to settle.

If the three independent multiplexers in the AM11-K are set for gains of 4, 16, and 64 and the multiplexer in the AD11-K is set for a gain of 1, a programmable gain data acquisition system can be configured. This is accomplished by connecting the same analog signal input to the corresponding input for all four multiplexers in the AM11-K and the AD11-K as shown in Figure 6-4. The result is 16 single-ended or 8 differential channels with gains of 1, 4, 16, and 64. The user software will select the appropriate sample and gain to convert.

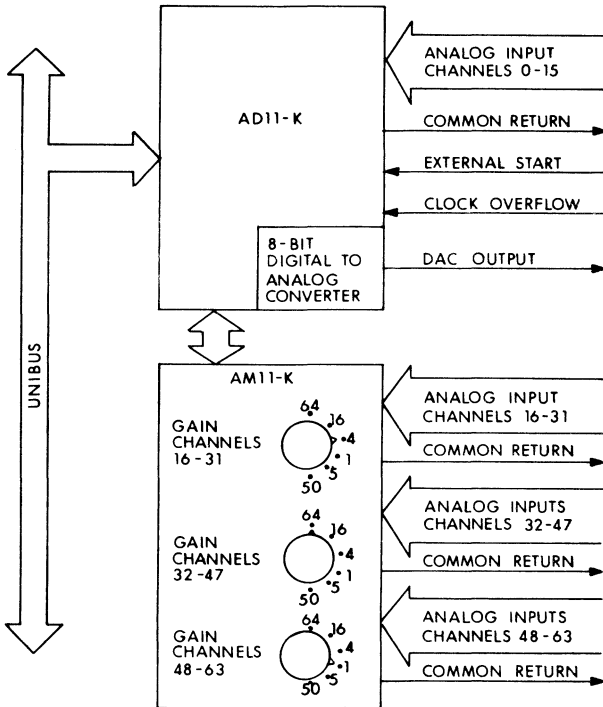


Figure 6-3 AM11-K BLOCK DIAGRAM

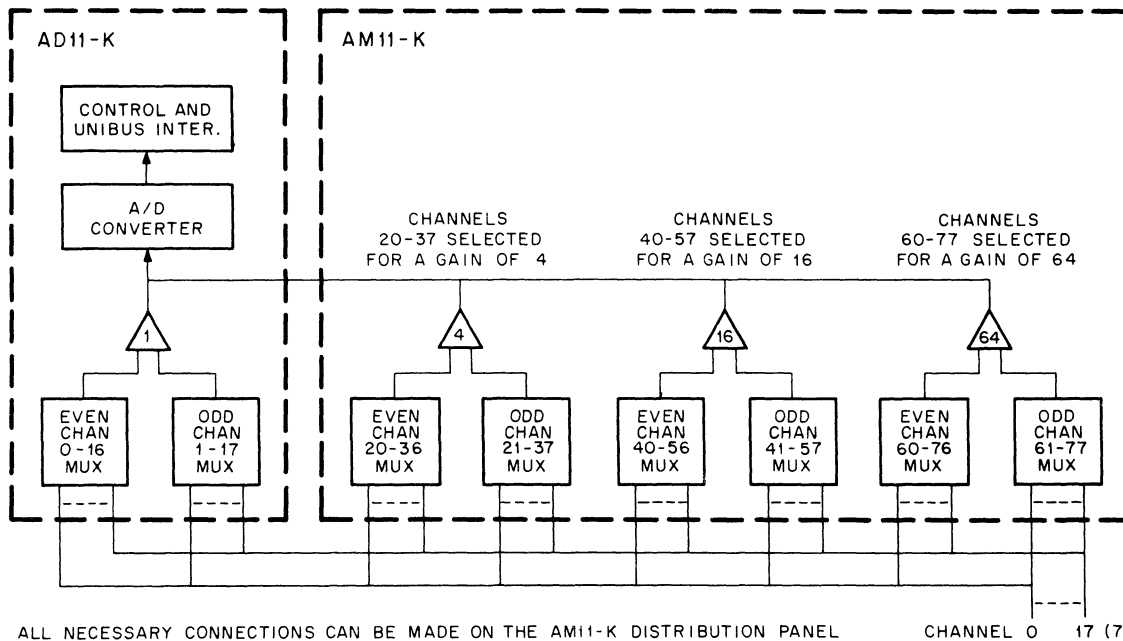


Figure 6-4 AD11-K/AM11-K PROGRAMMABLE GAIN BLOCK DIAGRAM

**SPECIFICATIONS**

**MECHANICAL**

Mounting code 5.25 in panel space

**PERFORMANCE**

Gain 1, 4, 5, 16, 50, 64 (switch-selectable in groups of 16 or 8 channels)

Channel input current 50 nA maximum

Channel input impedance 100 megaohms

Channel gain drift 25 ppm/°C maximum

Channel offset drift

RTI 5  $\mu$ V/°C maximum  
2  $\mu$ V/°C typical

RTO 0.5 mV/°C maximum  
0.25 mV/°C typical

Channel linearity (single-ended)  $\pm 0.05\%$  of full scale maximum  
 $\pm 0.025\%$  of full scale typical

Input slewing speed 2.5 Vdc/ $\mu$ s maximum

Interchannel settling error 2 Least Significant Bit

Crosstalk 80 dB down at 1 kHz (63 unselected channels into 1 selected channel)

Differential common mode rejection 70 dB from dc to 1 kHz at gain of 1; 90 dB from dc to 1 kHz at gain of 64

Throughput time (AM11-K with AD11-K) 42  $\mu$ s (10  $\mu$ s to select a channel plus 20  $\mu$ s for gain amplifier to settle, plus 12  $\mu$ s for A/D conversion)

**ELECTRICAL**

Current drawn 0.2 amps at +5 Vdc

Warmup time 5 minutes minimum

**ENVIRONMENTAL**

The AM11-K, used in conjunction with the AD11-K, conforms to the individual system's environmental specifications.

Operating temperature                      50°F–104°F (10°C–40°C)

Operating relative humidity                10%–90%  
(non-condensing)





**DR11-C**

The DR11-C is a general-purpose, digital interface between the PDP-11 UNIBUS and a user's peripheral. Under program control, the DR11-C transfers 16-bit parallel data between a PDP-11 system and an external device, such as another processor, peripheral, or user's application-specific device. The DR11-C is primarily used for interprocessor communication and for interfacing to foreign devices.

**FEATURES**

- Recoverable over-voltage protection
- Word or byte transfers
- 16 data lines, 2 control lines
- Maintenance cable for interface testing

**DESCRIPTION**

The DR11-C is an 18-line, general-purpose, digital interface used to transfer 16-bit parallel data between a PDP-11 UNIBUS and an external device under program control. A maintenance cable for testing the interface logic is also included. The DR11-C has 16 data lines (for transferring 16-bit parallel data) and 2 control lines (for transferring control and status information).

When used as an interprocessor buffer (IPB), the DR11-C allows data transfers between two processors. Interprocessor communication is accomplished by connecting one DR11-C to each processor UNIBUS and then cabling the two DR11-Cs together.

**OPERATION**

The DR11-C has three registers: the Control and Status register, the Output Buffer register, and the Input Buffer register. (Refer to the register section at the back of this book for register diagrams and bit definitions).

The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device. The output buffer register stores data read from the UNIBUS to be transferred to the user's device. The input buffer register stores data read from the user's device to be transferred to the UNIBUS.

Before beginning a data transfer operation, the processor addresses the DR11-C and reads the control and status register to determine whether it is to perform an input or output operation, and if an output operation, whether the data is to be transferred in words or bytes. Data inputs from the external device must be in 16-bit word format. Data outputs from the UNIBUS may be in either 16-bit word format or in 8-bit byte (either high- or low-byte) format.

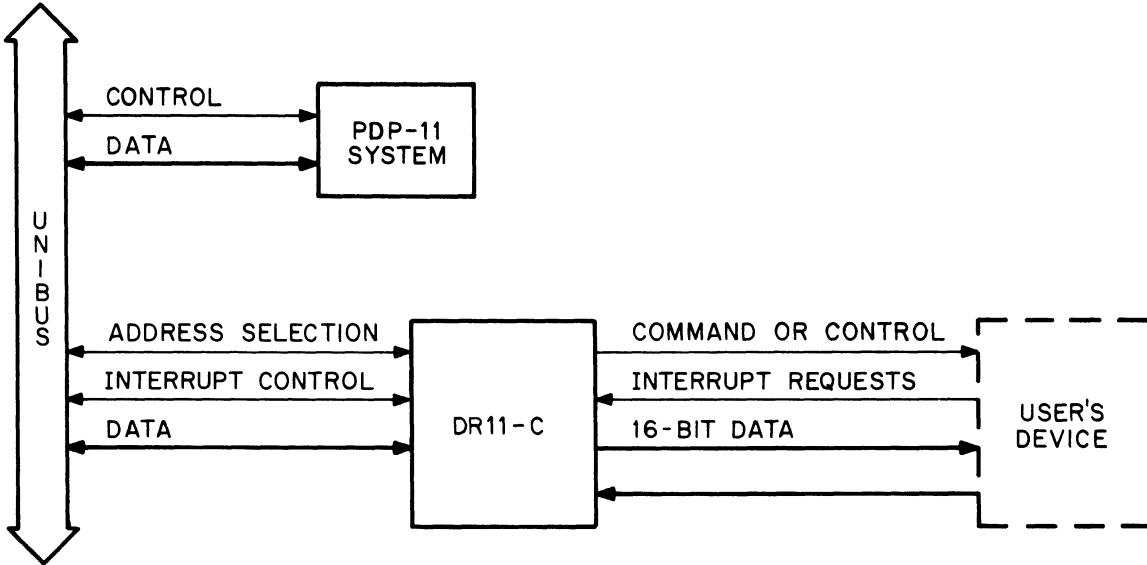


Figure 6-5 DR11-C BLOCK DIAGRAM

If an output operation is specified, data is transferred from the UNIBUS to the output buffer register. Once this register has been loaded, its contents are available to the external device via the 16 data output lines of the DR11-C, until the register is loaded with new data from the UNIBUS. Once the data has been transferred to the output buffer register, a NEW DATA READY control signal is sent to the user's device to indicate that data is available to be read.

When an input operation is specified, data is transferred from the user's device via the 16 data input lines of the DR11-C to the UNIBUS. Once the data has been transferred to the UNIBUS, a control signal, DATA TRANSMITTED, is sent to the user's device to indicate that the data has been read onto the UNIBUS.

Using the maintenance cable during an input or output operation permits checking of the interface logic since the input buffer register is loaded from the output buffer register rather than from the user's device. Thus, the same word loaded into the output register from the UNIBUS will appear in the input buffer, if the interface is functioning properly.

## **INTERRUPTS**

The DR11-C interrupt control logic permits the interface to gain control of the UNIBUS and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control while the interrupt bits are under the control of the user's device.

The DR11-C can generate an interrupt only if either the INTERRUPT ENABLE A bit or the INTERRUPT ENABLE B bit in the control and status register is set. Once INTERRUPT ENABLE A <06> is set, an interrupt request is generated whenever REQUEST A <07> is set. Once INTERRUPT ENABLE B <05> is set, an interrupt request is generated whenever REQUEST B <15> is set.

The DR11-C uses floating interrupt vector address assignments. The interrupt priority level is 5 and the interrupt vector address is 300. Note that the priority level can be changed with a priority plug and the vector address can be changed by switches in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

**SPECIFICATIONS**

Mounting code	1 quad slot
Current drawn	1.5 A at +5 Vdc

**PERFORMANCE**

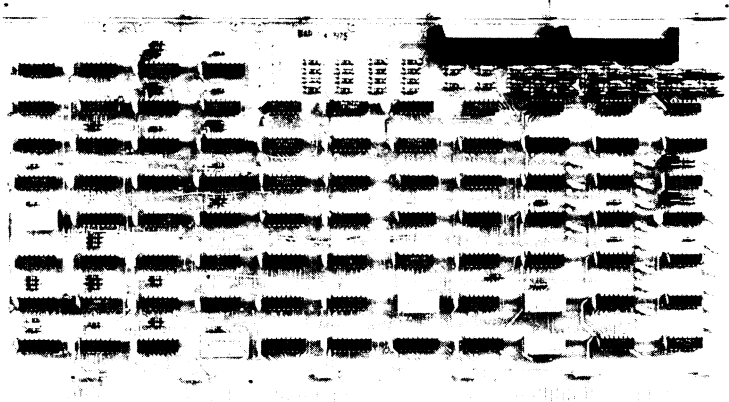
Data inputs	16-bit word from external device
Data outputs	16-bit word or 8-bit byte (either high or low) from the UNIBUS
Inputs	One standard TTL unit load; diode protection clamps to ground and +5 Vdc
Output signals	TTL levels capable of driving 8 unit loads except for the following: NEW DATA READY drives 30 unit loads, positive pulse, 400 ns wide unless width changed by an external capacitor DATA TRANSMITTED drives 30 unit loads, positive pulse, 400 ns wide unless width changed by an external capacitor INIT (initialize) —common signal on both connectors driven by one 30-unit load driver

**ENVIRONMENTAL**

The DR11-C conforms to the individual system's environmental specifications.

Operating temperature	50°F–104°F (10°C–40°C)
Operating relative humidity	10%–90% (non-condensing)





DR11-K

## **DR11-K**

The DR11-K is a general-purpose, digital input/output interface between the PDP-11 UNIBUS and a user's peripheral. Under program control, the DR11-K transfers 16-bit parallel data between a PDP-11 system and an external device, such as another processor, peripheral, or user's application-specific device. The DR11-K is primarily used to send and receive digital control signals to and from foreign devices.

## **FEATURES**

- 16 bidirectional data transfer lines, 4 control lines
- Recoverable over-voltage protection
- Word or byte transfers
- Two program-selectable modes of operation
- Maintenance cable for interface testing

## **DESCRIPTION**

The DR11-K is a 20-line, digital input/output interface used to transfer 16-bit parallel data between a PDP-11 UNIBUS and an external device under program control. A maintenance cable for testing the interface logic is also included. The DR11-K has 16 data lines (for transferring 16-bit parallel data) and 4 control lines (for transferring control and status information).

When used as an interprocessor buffer (IPB), the DR11-K allows data transfers between two processors. Interprocessor communication is accomplished by connecting one DR11-K to each processor UNIBUS and then cabling the two DR11-Ks together.

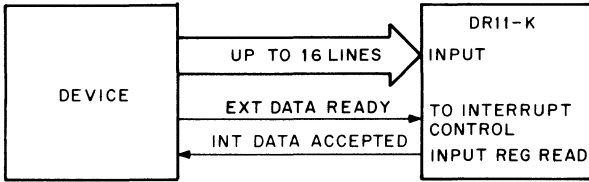
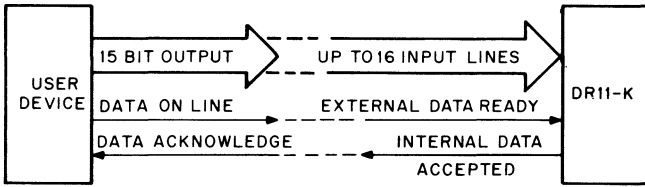
Using the maintenance cable during an input or output operation permits checking of the interface logic since the input buffer register is loaded from the output buffer register rather than from the user's device. Thus, the same word loaded into the output register from the UNIBUS will appear in the input buffer, if the interface is functioning properly.

## **OPERATION**

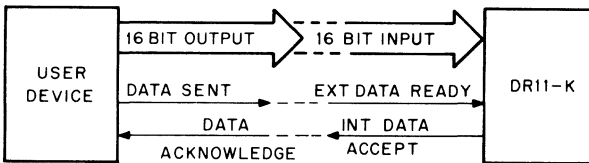
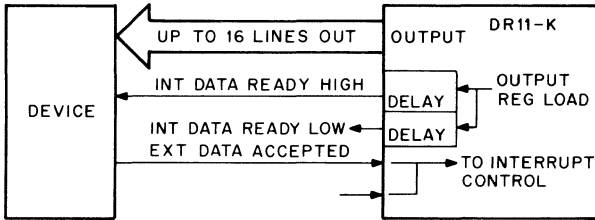
The DR11-K has three registers: the Status register, the Input register, and the Output register. (Refer to the register section at the back of this book for register diagrams and bit definitions).

The status register is used to enable interrupt logic, to provide user-defined command and status functions for the external device, and to generate maintenance interrupts. The output register stores data read

SENSOR I/O DEVICES



**INPUT BLOCK DIAGRAM**



**OUTPUT BLOCK DIAGRAM**

Figure 6-6 DR11-K BLOCK DIAGRAMS



from the UNIBUS to be transferred to the user's device. The input register stores data read from the user's device to be transferred to the UNIBUS.

Before beginning a data transfer operation, the processor addresses the DR11-K and reads the status register to determine whether it is to perform an input or output operation, and if an output operation, whether the data is to be transferred in words or bytes. Data inputs from the external device must be in 16-bit word format. Data outputs from the UNIBUS may be in either 16-bit word format or in 8-bit byte (either high- or low-byte) format.

If an output operation is specified, data is transferred from the UNIBUS to the output register. Once this register has been loaded, an INTERNAL HIGH DATA READY (indicating a high-byte data transfer) or an INTERNAL LOW DATA READY (indicating a low-byte data transfer) pulse is sent to the user's device to indicate that data is available to be read. When the external device has accepted the data, it sends an EXTERNAL DATA ACCEPTED signal to the DR11-K. If the OUTPUT INTERRUPT ENABLE bit in the status register is set when the DR11-K receives an EXTERNAL DATA ACCEPTED signal from the external device, the DR11-K sets the OUTPUT FLAG bit in the status register and generates an interrupt on the UNIBUS if the OUTPUT INTERRUPT ENABLE bit is set. The UNIBUS will clear the OUTPUT INTERRUPT ENABLE bit when it has accepted the interrupt.

When an input operation is specified, data is transferred from the user's device via the 16 data input lines of the DR11-K to either the DR11-K input register or the UNIBUS, depending on how the interrupt was generated. There are two ways of generating an interrupt: 1) by sending a control signal and 2) by setting the input register bits through their respective interrupt switches.

If interrupts are generated by the control lines, data can be read either directly off the data input lines of the DR11-K or from the DR11-K input register. When reading data from the DR11-K input register, note that the register must be cleared after each input operation. An EXTERNAL DATA READY signal is sent to the DR11-K by the external device and the DR11-K sets the INPUT FLAG bit in the status register and generates an interrupt on the UNIBUS if the INPUT INTERRUPT ENABLE bit in the status register is set. The UNIBUS will clear the INPUT INTERRUPT ENABLE bit when it has accepted the interrupt.

When the input register bits are set up to interrupt, the external device can generate an interrupt by setting any one of these input register bits. If the INPUT INTERRUPT ENABLE bit in the status register is set, an interrupt is generated on the UNIBUS. The UNIBUS clears the

INPUT INTERRUPT ENABLE bit once it has accepted the interrupt. Individual register bits can be cleared by performing a WRITE operation (using an appropriate mask) to the input register.

Each input line can be selected individually to interrupt the UNIBUS by simply presetting a micro switch mounted on the interface. The four most significant bits <15-12> have additional input buffer-setting capabilities. Hardware-selectable, these buffer bits can be set by a negative input transition, a positive input transition, or by either a positive or a negative transition. The bidirectional transition setting allows an interrupt to occur on an input change. This added feature of bits <12-15> was specifically designed for interfacing to devices such as the Coulter Model "S" Blood Counter.

### INTERRUPTS

The DR11-K interrupt control logic permits the interface to gain control of the UNIBUS and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control while the interrupt bits are under the control of the user's device.

The DR11-K can generate an interrupt only if either the INPUT INTERRUPT ENABLE bit or the OUTPUT INTERRUPT ENABLE bit in the status register is set. Once the INPUT INTERRUPT ENABLE bit is set, an interrupt request is generated whenever an EXTERNAL DATA READY control signal is received by the DR11-K or a transition occurs on any of the individual data input lines. Once the OUTPUT INTERRUPT ENABLE bit is set, an interrupt request is generated whenever an EXTERNAL DATA ACCEPTED signal is received by the DR11-K.

The DR11-K uses floating interrupt vector address assignments. The interrupt priority level is 4 and the interrupt vector address is 300 (input) and 304 (output). Note that the priority level can be changed with a priority plug and the vector address can be changed by switches in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

### SPECIFICATIONS

Mounting code	One hex slot
Current drawn	2.5 A at +5 Vdc maximum

### PERFORMANCE

Data inputs	16-bit word from external device
-------------	----------------------------------

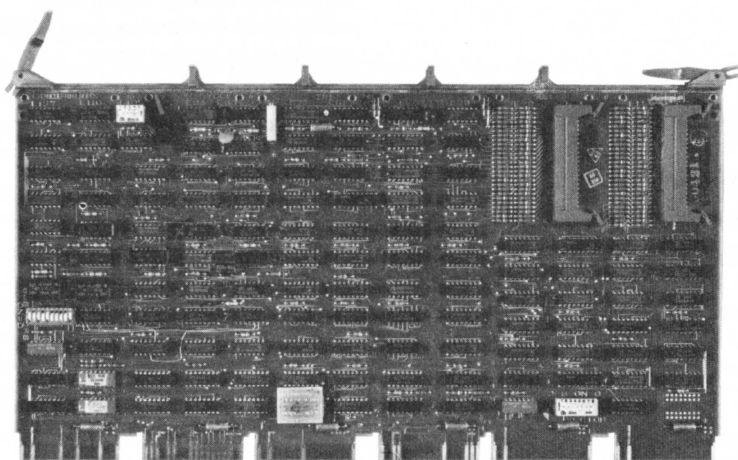
## SENSOR I/O DEVICES

Data outputs	16-bit word or 8-bit byte (either high or low) from the UNIBUS
Inputs	TTL compatible; over-voltage protection from -10 Vdc to +15 Vdc by 47 ohm fusible resistors that open when current exceeds 250 mA; hysteresis for high and low thresholds
Outputs	All driven by open collector logic; over-voltage protected and current-protected by fuses that open when current exceeds 250 mA when in a zero state

### ENVIRONMENTAL

The DR11-K conforms to the individual system's environmental specifications.

Operating temperature	50°F–104°F (10°C–40°C)
Operating relative humidity	10%–90% (non-condensing)



DR11-W

### **DR11-W**

The DR11-W is a general purpose, direct memory access (DMA) interface to the PDP-11 UNIBUS or VAX UNIBUS Adapter (UBA). The DR11-W moves data directly between memory and the UNIBUS or UBA to and from the user's peripheral.

### **FEATURES**

- Word or byte transfers
- Programmed or direct memory access (DMA) block transfers
- Burst data transfers
- User-controlled transfer rates up to memory speed
- Maintenance cable for interface testing

### **DESCRIPTION**

The DR11-W is a 53-line, direct memory access (DMA) interface to the PDP-11 UNIBUS or VAX UBA, which allows the user to control data transfers between the host processor and a peripheral. A maintenance cable for testing the interface logic is also included. The DR11-W has 32 data lines (for transferring 16-bit parallel data) and 21 control lines (for transferring control and status information).

When used as an interprocessor buffer (IPB), the DR11-W allows data transfers between two processors. Interprocessor communication is accomplished by connecting one DR11-W to each processor UNIBUS or UBA and then cabling the two DR11-Ws together.

### **OPERATIONAL MODES**

The DR11-W has two functional modes of operation, DR11-B mode and DR11-W mode. In DR11-B mode, the DR11-W is both functionally and software compatible with the DR11-B. DR11-W mode provides additional error condition monitoring and enables the interprocessor link capability. Programming the device in DR11-W mode is slightly different from DR11-B mode. For PDP-11 systems, the DR11-W is supported in both modes with diagnostics for the user's device and the interprocessor link applications. As with the DR11-B, the user is responsible for supplying the interface software. For VAX systems, the DR11-W is supported in DR11-W mode only with both diagnostics and VAX/VMS operating system support.

### **OPERATION**

The DR11-W has six registers: the Control and Status register, the Error and Information register, the Word Count register, the Bus Address register, the Input Data register, and the Output Data register. (Refer to the register section at the back of this book for register diagrams and bit definitions).

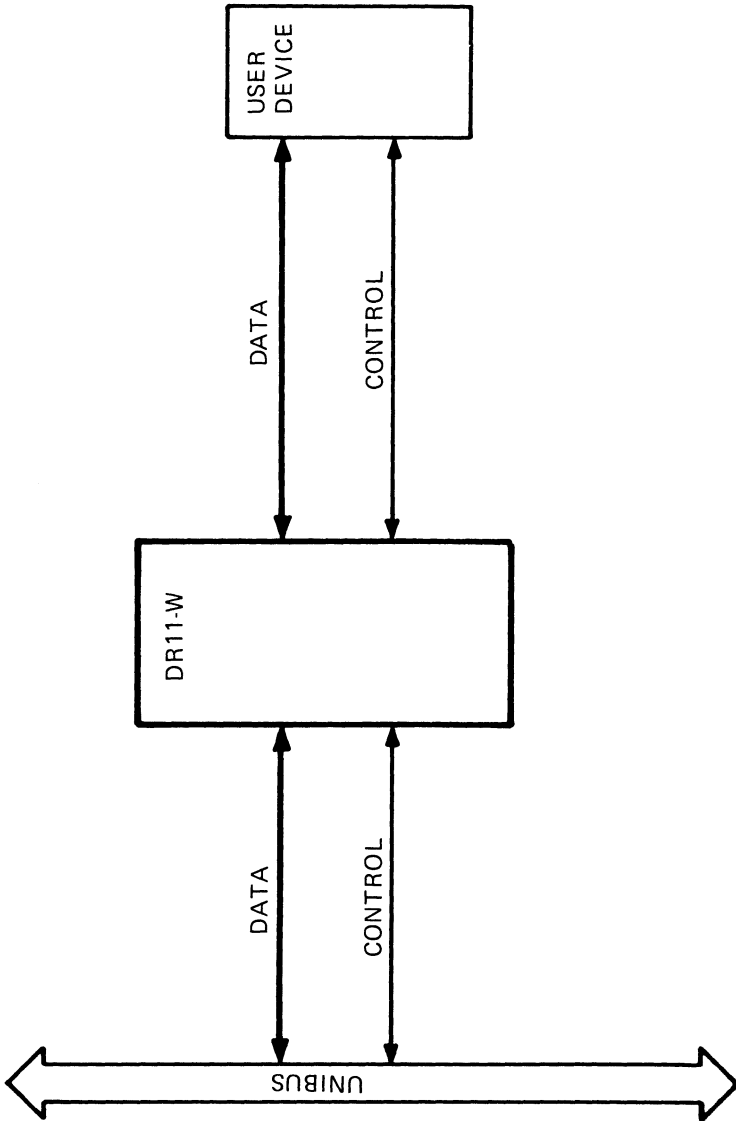


Figure 6-7 DR11-W BLOCK DIAGRAM

The control and status register is used to enable interrupt logic, to provide user-defined command and status functions for the external device, and to provide error information. The error and information register provides additional error recording such as BURST DATA LATE, etc. The word count register allows the user to predefine the number of transfers to be performed. The bus address register allows the user to define the starting address where the transfer is to begin. The output data register stores data read from the UNIBUS to be transferred to the user's device. The input data register stores data read from the user's device to be transferred to the UNIBUS.

Before beginning a data transfer operation, the processor addresses the DR11-W and loads the control and status register to perform an input or output operation. When the control and status register is loaded to perform an output operation, the processor also specifies whether the data is to be transferred in words or bytes. Data inputs from the external device must be in 16-bit word format. Data outputs from the UNIBUS may be in either 16-bit word format or in 8-bit byte (either high- or low-byte) format. The processor then loads the bus address register with the starting memory address where the data transfer is to begin and the word count register with the two's complement of the number of data transfers to be performed. Finally, the GO bit in the control and status register is loaded to initiate the transfer.

If an output operation is specified, data is transferred from the UNIBUS to the DR11-W output data register. Once this register has been loaded, its contents are available to the external device until the register is loaded with new data from the UNIBUS. Once the data has been transferred to the output data register and the BUSY line is unasserted, the data is available to be read by the external device.

When an input operation is specified, data is transferred, along with user-defined function bits, from the user's device to the DR11-W. The user-defined function bits are loaded into the control and status register and the data is loaded into the input data register. Data from the input data register is then transferred to the UNIBUS. The data transfer to the UNIBUS is completed once the BUSY line is unasserted.

Using the maintenance cable during an input or output operation permits checking of the interface logic since the input data register is loaded from the output data register rather than from the user's device. Thus, the same word loaded into the output data register from the UNIBUS will appear in the input data register, if the interface is functioning properly.

## INTERPROCESSOR LINKS

The DR11-W can be used to form a DMA parallel-data transfer link between two computer systems. It can be connected to another DR11-W or to a DRV11-B. The link operates in half-duplex mode, i.e. although the link has the capability of transferring data in both directions, it is dedicated to transferring data in only one direction at a given time.

Interprocessor links can operate in three different transfer modes: word, block, and burst (burst is limited to DR11-W/DR11-W links only). In word mode, information can be passed between two computers, one word at a time, by an interrupt-driven program. In block and burst modes, the interprocessor link transmits a block of consecutive locations from the memory in one computer to the memory in another. The link accomplishes this by using DMA transfers in each computer. In block mode, the DR11-W must obtain and release the UNIBUS for each data transfer it makes. This operation allows other devices on the UNIBUS to interleave transfers with the DR11-W. In burst mode, the DR11-W obtains control of the UNIBUS and holds in for either two-cycle or N-cycle data transfers. The selection of the transfer mode must ensure operational compatibility with the overall system environment.

## INTERRUPTS

The DR11-W interrupt control logic permits the interface to gain control of the UNIBUS and perform program interrupts to specific vector addresses. The interrupt enable bit is under program control while the interrupt bits are under the control of the user's device.

The DR11-W can generate an interrupt only if the INTERRUPT ENABLE bit in the control and status register. Once INTERRUPT ENABLE <06> is set, an interrupt request is generated whenever any of the following bits in the control and status register is set: ERROR <15>, NON-EXISTENT MEMORY <13>, ACLO <11>, MULTI-CYCLE REQUEST <12>, and PARITY ERROR <10>. In interprocessor link mode, FUNCTION 2 <02> will also generate an interrupt.

The DR11-W uses floating interrupt vector address assignments. The interrupt priority level is 5 and the interrupt vector address is 124 for the first DR11-W. Vector addresses for additional DR11-Ws are assigned by the user. Note that the priority level can be changed with a priority plug and the vector address can be changed by switches in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.



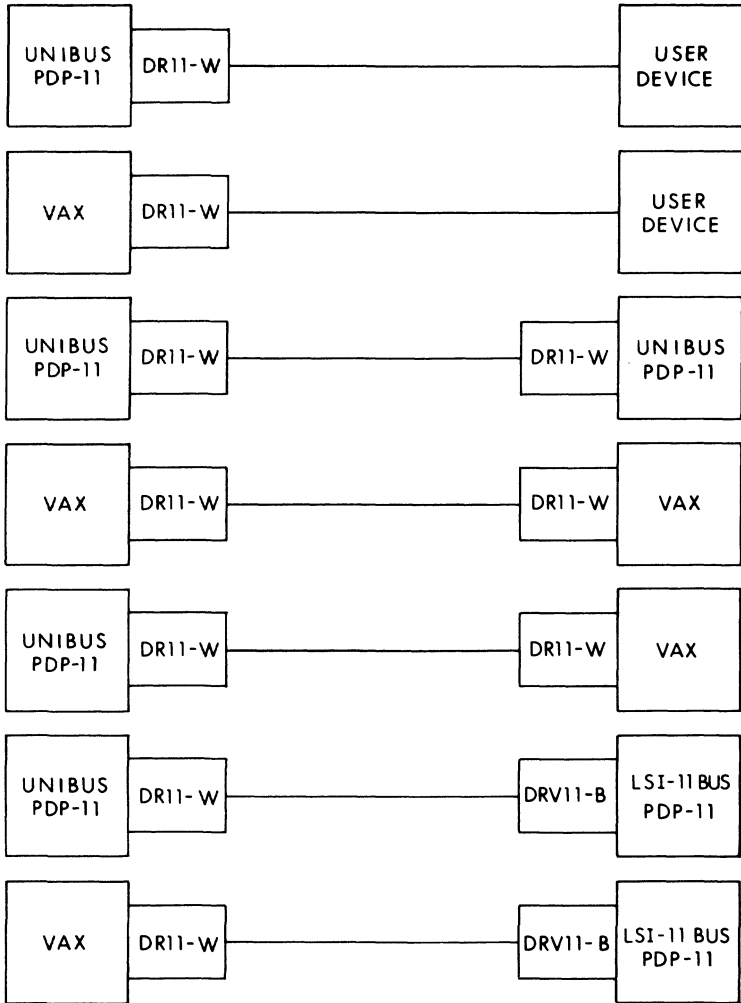


Figure 6-8 INTERFACE CONFIGURATIONS



**IB11**

The IB11 is a 16-line, IEEE standard instrument bus interface that allows test and measurement instruments that are IEEE instrument bus compatible to be interfaced to the PDP-11 UNIBUS. Typical test and measurement instruments, such as digital counters, frequency synthesizers, digital multimeters, and programmable power supplies, are designed to be compatible with the IEEE 488-1975 Instrument Bus Standard. By interfacing these IEEE instrument bus compatible devices to the PDP-11 UNIBUS, the IB11 provides an easy-to-use, inexpensive, programmable instrumentation system.

**FEATURES**

- Instrument bus compatible with IEEE Standard 488-1975
- Supports UNIBUS cable length up to a total of 65.6 ft (20 m)
- Supports a maximum of 15 devices on the instrument bus
- Interrupt-driven interface
- Self-diagnostic routines
- Support for FORTRAN-callable subroutines under the RT-11 operating system

**DESCRIPTION**

The IB11 IEEE standard instrument bus interface consists of all the necessary cables and instrument connectors to interconnect a system. The cables are terminated with a standard connector to mate with any IEEE standard instrument bus compatible instrument or device. The IB11 is available in three different versions depending on the software distribution media. All versions of the IB11 come with the necessary equipment for mounting in a BA11-K box. The IB11-KE version software is distributed on the RK05, the IB11-KQ version software is distributed on the RL01, and the IB11-KY version software is distributed on the RX01/RX02 diskette.

**OPERATION**

The IB11 has two registers: the Instrument Bus Status register and the Instrument Bus Data register. (Refer to the register section at the back of this book for register diagrams and bit definitions).

System devices may function as talkers, listeners, controllers, or a combination of all three. A controller is capable of controlling talkers and listeners connected to the instrument bus. Only one controller may be active at a time, and is designated the controller-in-charge. The IB11 is usually designated controller-in-charge, and as such schedules all device addressing, device polling, commands, and data byte transfers. A listener receives commands and data from the instrument



bus. More than one listener may be active at a time. A talker receives commands and transfers data via the instrument bus. Only one talker may be active at a time.

It is not necessary for each device on the instrument bus to be capable of responding to all of the lines. Each device can be designed to respond only to those lines that are relevant to its function on the bus.

The instrument bus transfers data and commands asynchronously over 16 signal lines. The eight data lines comprise an eight-bit bidirectional data bus. As the system controller, the IB11 transfers commands via the Data Input/Output (DIO) lines as 7-bit ASCII characters (the DIO8 line is not used for command transfers). The actual commands and the sequence in which they are issued are completely under the control of the PDP-11 software being executed.

The eight remaining lines perform control and handshaking functions. Data transfer between the devices is coordinated by the three data transfer control or handshake lines: Data Valid (DAV), Not Ready For Data (NRFD), and Not Data Accepted (NDAC). These lines operate sequentially, i.e. no step in the sequence can be initiated until the previous step has been completed.

The five bus management message lines or control lines are as follows:

- Attention (ATN) is used by the IB11 to transfer commands over DIO lines. It causes active talkers to become inactive.
- Interface Clear (IFC) is asserted only by the IB11 as "master clear" and causes all devices to return to idle state within 100  $\mu$ s.
- Remote Enable (REN) is used by the IB11 to enable remote operation or is negated for local operation. Local mode devices may respond to instrument bus transmissions that do not conflict with local control functions.
- End Or Identify (EOI) is used by the IB11 or by an active talker to indicate the end of a multiple-byte transfer sequence. By asserting EOI and ATN, the IB11 can conduct a parallel poll.
- Service Request (SRQ) is used by an active device on the instrument bus requiring the attention of the IB11.

## **INTERRUPTS**

The IB11 can generate an interrupt only if the INTERRUPT ENABLE bit in the instrument bus status register is set. Once the INTERRUPT ENABLE bit is set, interrupts occur under program control.

The IB11 uses floating interrupt vector address assignments. The interrupt priority level is 6 and the interrupt vector address is 420. Note that the priority level can be changed with a priority plug and the

vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## SPECIFICATIONS

### MECHANICAL

Mounting code	1 quad slot, 1 SU
Height	5.2 in (13.2 cm)
Length	8.9 in (22.8 cm)
Width	0.5 in (1.3 cm)

### ELECTRICAL

Current drawn	3.5 A at +5 Vdc
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### PERFORMANCE

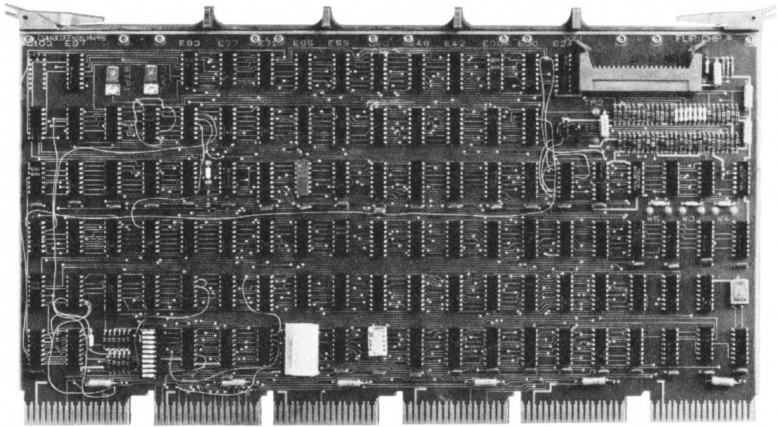
Data Rate	9.2 KB/s (talker), 8 m cable length 5.8 KB/s (listener), 8 m cable length
Address capability	Maximum of 1 talker, and 14 listeners at a time
Primary addresses	31 talker, 31 listener
Secondary (2-byte) addresses	961 talker, 961 listener

### ENVIRONMENTAL

The IB11 conforms to the individual system's environmental specifications.

Operating temperature	50°F–104°F (10°C–40°C)
Operating relative humidity	10%–90% (non-condensing)

*SENSOR I/O DEVICES*



**KW11-K**



**KW11-K**

The KW11-K is a dual-programmable, realtime clock supported by UNIBUS PDP-11 systems on the UNIBUS or on the LPA11-K bus and by VAX-11 systems only on the LPA11-K bus. The primary application of the KW11-K is to provide the time base for digital-to-analog converters, such as the AA11-K, analog-to-digital converters, such as the AD11-K, and digital I/O modules, such as the DR11-K, the DR11-W, and the DR11-C. The KW11-K is also used to provide the timing pulse for external devices.

**FEATURES****CLOCK A**

- Four modes of operation
- Two external inputs (Schmitt triggers)
- Eight program-selectable clock rates
- Five clock frequencies

**CLOCK B**

- Repeated interval mode of operation
- One external input (Schmitt trigger)
- Seven program-selectable clock rates
- Five clock frequencies

**DESCRIPTION**

The KW11-K dual-programmable realtime clock option consists of two realtime clocks: clock A and clock B. Clock A is a 16-bit programmable realtime clock that accurately measures and counts intervals of time and events. It can be used for processor synchronization to external events, to generate events, such as an A/D conversion at programmed intervals, and to generate events synchronized to an external event input, such as a signal generator. Clock A operates in one of four programmable modes: single interval, repeated interval, external event timing, and external event timing from zero base. Clock A can be program-selected to operate at one of the following eight clock rates: one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), an external input (Schmitt trigger one), line frequency, and the overflow of clock B (allowing a further subdivision of clock A input frequency selections).

Clock B is an 8-bit programmable real-time clock that accurately times intervals and events. It can be used for generating interrupts at programmed intervals, for generating events, such as an A/D conversion at programmed intervals, and for providing an input frequency to clock A. Clock B operates in one mode only: repeated interval mode.

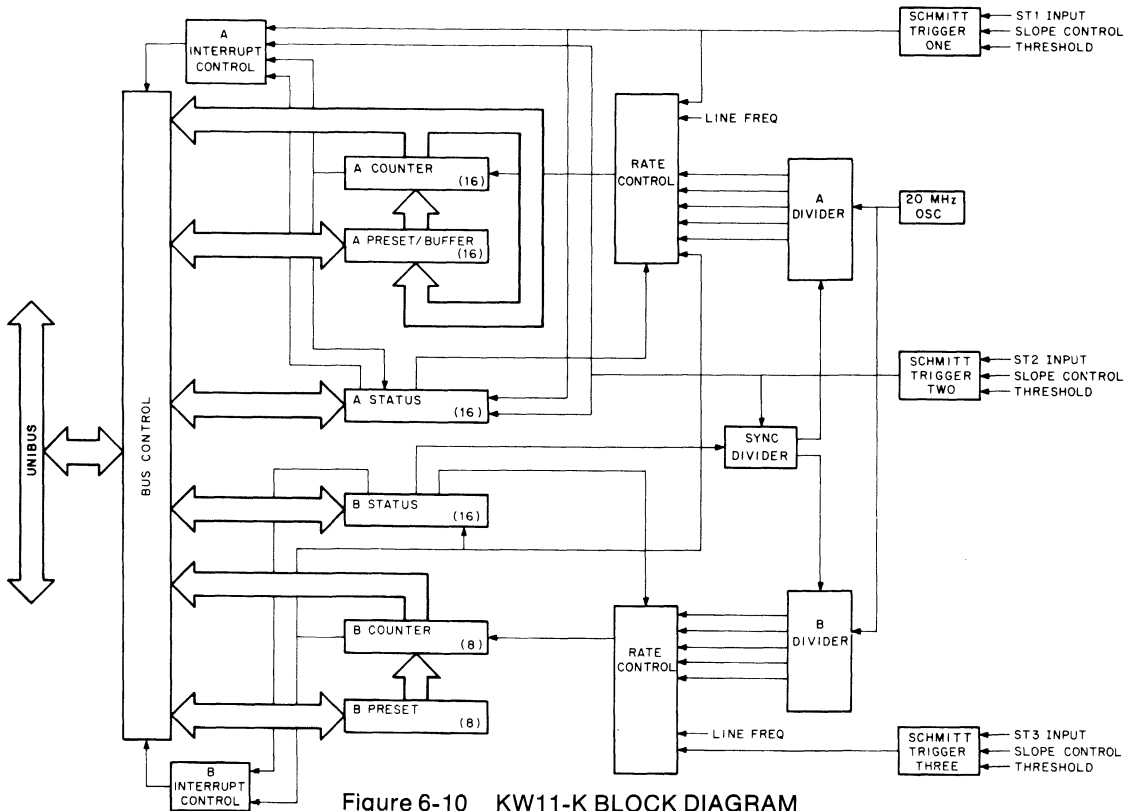


Figure 6-10 KW11-K BLOCK DIAGRAM

Clock B can be program-selected to operate at one of the following seven clock rates: one of five crystal-controlled frequencies (1 MHz, 100 kHz, 10 kHz, 1 kHz and 100 Hz), an external input (Schmitt trigger three), line frequency, and stop frequency.

## OPERATION

The KW11-K dual-programmable realtime clock has six registers: the A Status register, the A Preset/Buffer register, the A Counter register, the B Status register, the B Buffer register, and the B Counter register. (Refer to the register section at the back of this book for applicable register diagrams and bit definitions.)

Clock A is program-controlled by the A status register and clock B is program-controlled by the B status register. The A and B Counter registers keep track of the number of clock pulses that have elapsed since the clock was initiated. The A Preset/Buffer register and the B Buffer register store the timing data for the A and B clocks respectively.

The KW11-K has three Schmitt trigger inputs with threshold and slope control. An external ST1 (Schmitt trigger one) input is used 1) to start clock A, 2) as a counting function for clock A, and 3) to generate an interrupt. An external ST2 (Schmitt trigger two) is used by clock A on overflow to transfer the contents of the A Counter register into the A Preset/Buffer register. An external ST3 (Schmitt trigger three) is used 1) to start clock B, and 2) as a counting function for clock B.

## INTERRUPTS

The KW11-K can generate an interrupt only if either the MODE FLAG INTERRUPT ENABLE bit in the A Status register, the B OVERFLOW ENABLE bit in the B Status register, or the ST1 INTERRUPT ENABLE bit in the A Status register is set. Once the MODE FLAG INTERRUPT ENABLE bit is set, an interrupt request is generated whenever clock A overflows. Once the B OVERFLOW ENABLE bit is set, an interrupt request is generated whenever clock B overflows. Once the ST1 INTERRUPT ENABLE bit is set, an interrupt request is generated whenever an ST1 (Schmitt trigger one) event occurs.

The KW11-K uses floating interrupt vector address assignments. The interrupt priority level is 6 and the interrupt vector address is 344. Note that the priority level can be changed with a priority plug and the vector address can be changed by jumpers in the interrupt control logic. However, any DIGITAL programs or other software referring to the priority level or interrupt vector address must also be changed if the priority plug or the vector address is changed.

## SENSOR I/O DEVICES

### **SPECIFICATIONS**

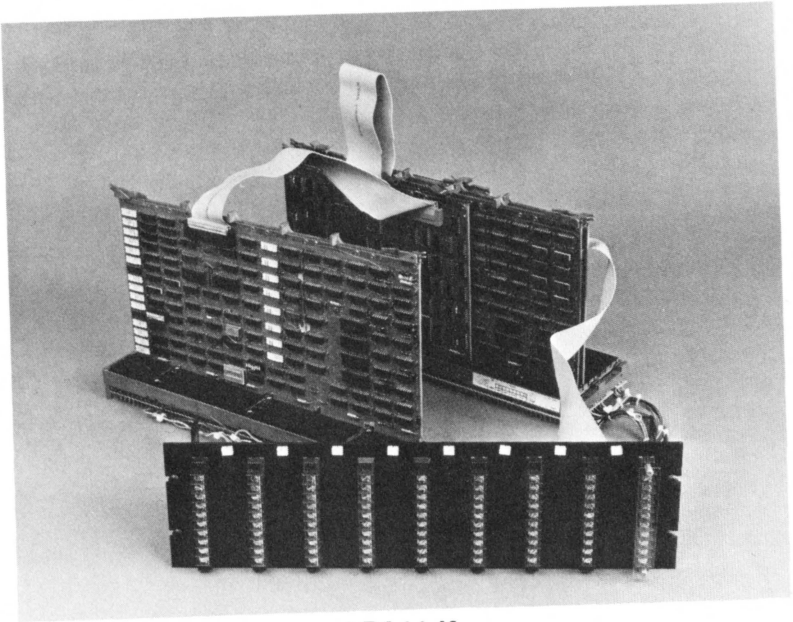
Mounting code	1 hex slot (UNIBUS or LPA11-K bus)
Current drawn	3 A at +5 Vdc maximum

### **ENVIRONMENTAL**

The KW11-K conforms to the individual system's environmental specifications.

Operating temperature	50°F–104°F (10°C–40°C)
Operating relative humidity	10%–90% (non-condensing)





LPA11-K

## **LPA11-K**

The LPA11-K is an intelligent, high-speed, direct memory access (DMA) subsystem designed for use with DIGITAL's laboratory data acquisition I/O devices. It is intended to be used in a variety of laboratory applications where I/O rates are in excess of 2-5 KHz and when there is a requirement for concurrent data processing. The LPA11-K transfers data directly between main memory and the UNIBUS or UBA to and from the I/O devices connected to it.

## **FEATURES**

- Microprocessor-controlled
- Direct Memory Access (DMA) data transfers
- Software support of up to eight concurrent tasks
- Supported by FORTRAN- and MACRO-callable subroutines
- Silo (first-in/first-out) memory internal to the LPA11-K subsystem allows data to be transferred continuously
- Automatic buffer switching eliminates data loss

## **DESCRIPTION**

The LPA11-K subsystem consists of an intelligent controller with two microprocessors, a UNIBUS interface, and a library of FORTRAN- and MACRO-callable subroutines. The LPA11-K transfers 16-bit data between main memory and the UNIBUS or UBA to specified analog-to-digital converters, digital-to-analog converters, and digital input and output interfaces. Any of the devices connected to the LPA11-K may be shared by multiple users. Because data transfers are controlled by the microprocessor within the LPA11-K, interrupt service routines are not required, allowing more efficient use of the central processor.

In situations where high data throughput is required, multiple LPA11-Ks can be configured on a system. Although up to four LPA11-Ks are usually supported by a UNIBUS PDP-11 system, the total number depends on the individual application. VAX-11/780 systems support two LPA11-K subsystems and VAX-11/750 systems support one LPA11-K subsystem.

## **OPERATION**

The LPA11-K subsystem has two independent microprocessors which allow it to sample and transfer data between the host processor's main memory and laboratory data acquisition I/O devices without involving the host processor. The first microprocessor is the master and the second microprocessor is the slave. The host processor may be either a PDP-11 UNIBUS system or a VAX system and is responsible for

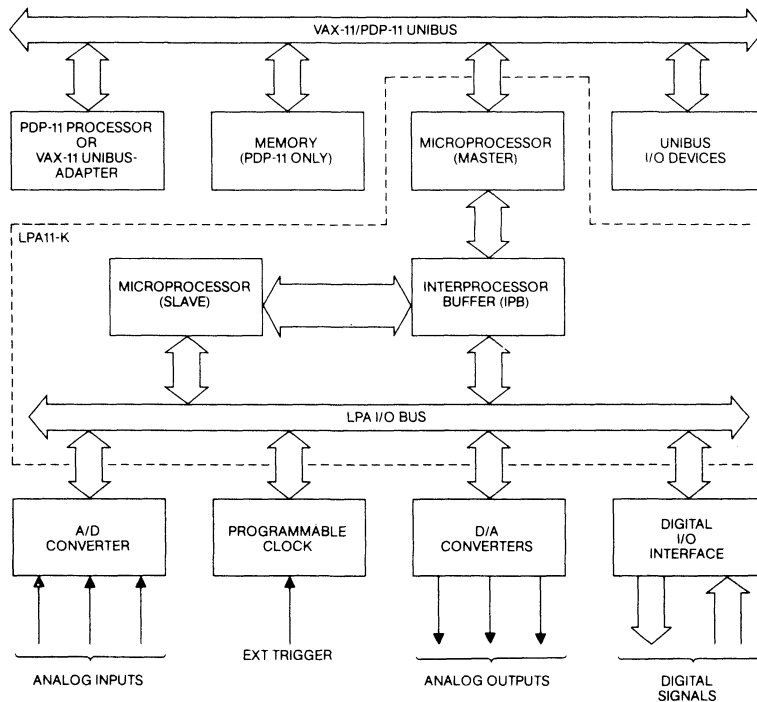


Figure 6-11 LPA11-K BLOCK DIAGRAM



initializing the LPA11-K, sending requests to start and stop sampling of data, and handling errors and other status conditions. The master microprocessor connects directly to the UNIBUS and communicates with main memory by DMA. It is responsible for all transactions between the host processor and the LPA11-K. These include control information as well as storage and retrieval of all data from main memory. The slave microprocessor controls the laboratory data acquisition I/O devices. When a START DATA ACQUISITION command is received from the master microprocessor, the slave microprocessor then sends or receives a continuous stream of data until a STOP command is received or a fatal error condition occurs.

The master and slave microprocessors are connected by the intermicroprocessor buffer (IPB) module. This module buffers all transactions between the microprocessors with two 64-byte, first-in/first-out silo registers. This allows the two microprocessors to operate asynchronously and independently. The IPB also provides the necessary control signals for the slave microprocessor to communicate with the laboratory data acquisition I/O devices.

All input or output data transfers are driven and synchronized by the programmable realtime clock required by the LPA11-K subsystem. If the clock is not running, data transfers cannot occur. Note that the programmable realtime clock must be ordered separately from the LPA11-K.

### **OPERATIONAL MODES**

The LPA11-K can operate in two exclusive modes: dedicated mode and multirequest mode. In dedicated mode, the LPA11-K performs high-speed input or output for a single user. In multirequest mode, the LPA11-K allows up to eight simultaneous tasks to be performed at independent rates from any combination of the supported devices. Each user programs the LPA11-K as if they had sole access to it. Starting and stopping one user's requests does not affect the other active LPA11-K requests.

In dedicated mode, one user at a time can sample from an analog-to-digital converter or output to a digital-to-analog converter. Two analog-to-digital converters can be controlled simultaneously. Sampling is initiated by overflow of the programmable realtime clock or by an external event. Two sampling algorithms are implemented. The first algorithm, at each overflow, samples both analog-to-digital converters in parallel, allowing two channels to be sampled simultaneously. The maximum single channel rate per analog-to-digital converter is 75,000 samples per second or an aggregate of 150,000 samples per second for two analog-to-digital converters. The maximum multiple channel

rate is 40,000 samples per second per channel (80,000 aggregate). The second algorithm samples the two analog-to-digital converters on an interleaving basis, beginning with the first, whose sampling begins on alternate clock overflows. One four-channel digital-to-analog converter can be controlled as well. Sampling is initiated under micro-code control by an overflow of the programmable realtime clock.

**DEDICATED MODE ANALOG-TO-DIGITAL SAMPLING  
AGGREGATE THROUGHPUT RATES (IN KHZ)**

	<b>AD11-K</b>	<b>AD11-K with AM11-K</b>	<b>AR11</b>
<b>SINGLE A-TO-D</b>			
Single	75	75	35
Sequential	40	23	30
Random	40	23	30
<b>DUAL A-TO-D SERIAL MODE</b>			
Single	100*	100*	N/A
Sequential	80	46	N/A
Random	70	46	N/A
<b>DUAL A-TO-D PARALLEL MODE</b>			
Single	2 × 75	2 × 75	N/A
Sequential	2 × 40	2 × 23	N/A
Random	2 × 40	2 × 23	N/A

Multirequest mode supports sampling from all device types. Up to eight user tasks can be active simultaneously. Each task's sampling rate is a user-specified multiple of the common programmable realtime clock rate. Independent rates can be maintained for each task. Each task requests a specific device type or combination of device types. When the DR11-K is used with the LPA11-K, sampling can be synchronized with an external event or through internal hardware con-

\* Obtained by wiring user signal to same channel on both A-to-Ds.

trol lines. This capability allows 16-bit parallel data to be transferred at a rate determined by the external device.

Each user task sampling analog or digital channels can request that the data be time-stamped with a value from an internal clock. This allows an application program to mark when each sample was taken. Event-marking mode marks each sample with a one-bit flag indicating whether a user-supplied external event has occurred. This allows a user to examine data at positive or negative time in relation to the external event.

In multirequest mode, the throughput of data is determined by the number and type of requests. The aggregate throughput rate for all user tasks is 12-15,000 samples per second depending on the sampling mode.

### **CHANNEL ADDRESS SELECTION**

In both dedicated and multirequest modes, there is a need to specify the address of the next channel to be sampled. In the case of analog input, the channel address specifies which multiplexer channel to enable. In the case of digital I/O, the channel address specifies which digital I/O word to access. The LPA11-K uses three types of channel address selection: single-channel mode, sequential-channel mode, and random-channel mode.

In single-channel mode, the LPA11-K repeatedly samples the same channel. This is the simplest mode and allows the highest throughput.

In sequential-channel mode, the LPA11-K calculates the address of the next channel by adding a user-supplied positive or negative increment to the current channel. When the last channel is sampled, the LPA11-K resets the current channel to the starting channel. This allows the user to scan a preselected range of channels.

In random-channel mode, the LPA11-K determines the address of the next channel by accessing a user-supplied table in the host processor's main memory. This is the most general of the channel address selection modes since channels can be sampled in any sequence, but results in a lower aggregate throughput rate.

### **STORAGE OF DATA IN MAIN MEMORY**

In dedicated mode, and for each of the possible eight user's tasks in multirequest mode, up to eight independent buffer addresses can be specified for each user. The LPA11-K maintains each user's buffers separately and the size of each set of buffers for a given user is the same (specified at the beginning of each request). When one buffer is full, the LPA11-K automatically switches buffers without any interaction with the user's program.

**OPERATING MODE SUMMARY**

<b>FEATURES</b>	<b>DEDICATED MODE</b>	<b>MULTIREQUEST MODE</b>
Number of independent user-operations (requests)	1 request	8 requests
Aggregate throughput to memory	100 KHz with two A-to-Ds in serial 2 × 75 KHz with two A-to-Ds in parallel (aggregate 150 KHz)	12-15 KHz maximum
Supported options	1 KW11-K 2 AD11-Ks 2 AM11-Ks 1 AR11 1 AA11-K	All options under dedicated mode plus 5 DR11-Ks
Operations	High-speed A/D conversions or D/A conversions	Simultaneous A/D conversions, D/A conversions, digital I/O, time-stamping, event-marking, digital trigger
Rate selection	Single rate triggered by programmable clock or external event	Individual rates per request (maximum of 8) as submultiples of realtime clock rate

**FORTRAN-CALLABLE SUBROUTINES**

A library of FORTRAN-callable subroutines included with the LPA11-K subsystem provide functions for request initialization, I/O control, buffer control, utilities for floating point conversions, computing clock-rate and preset, and converting an unsigned integer to a real constant. Each FORTRAN call contains arguments that specify the request parameters. Note that these FORTRAN-callable subroutines are also MACRO-callable.

**FORTRAN-CALLABLE SUBROUTINES FOR THE LPA11-K**

ADSWP	Initiates synchronous A/D sweep
CLOCKA	Sets clock A rate
CLOCKB	Controls clock B
CVADF	Converts A/D input to floating point
DASWP	Initiates synchronous D/A sweep
DISWP	Initiates synchronous digital input sweep
DOSWP	Initiates synchronous digital output sweep
FLT16	Converts unsigned integer to a real constant
IBFSTS	Gets buffer status
IGTBUF	Returns buffer number
INXTBF	Sets next buffer
IWTBUF	Waits for buffer
LAMSKS	Sets mask buffer
RLSBUF	Releases data buffer
RMVBUF	Removes buffer from device queue
SETADC	Sets channel information
SETIBF	Sets array for buffered sweep
STPSWP	Stops sweep
XRATE	Computes clock rate and preset

# SENSOR I/O DEVICES

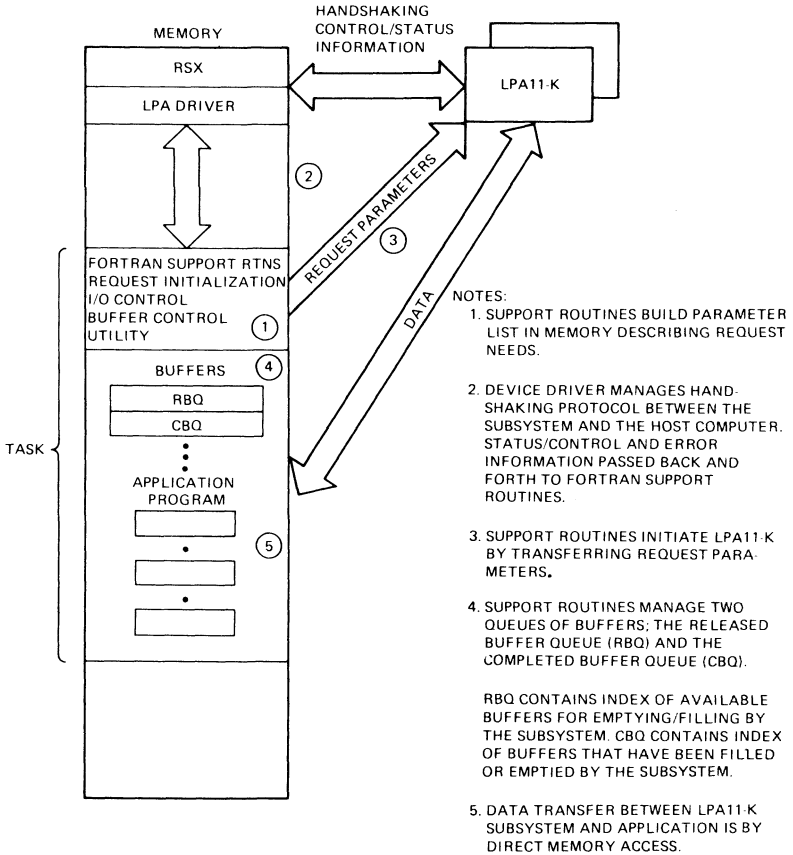


Figure 6-12 LPA11-K SUBSYSTEM SOFTWARE STRUCTURE

**I/O BUS DEVICE/CLOCK ADDRESSES**

<b>DEVICE TYPE</b>	<b>I/O BUS CSR ADDRESS</b>	<b>INTERRUPT VECTOR ADDRESS</b>
AD11-K Analog- to-Digital Converter No. 1	770400	340
AD11-K Analog- to-Digital Converter No. 2	770440	400
KW11-K Programmable Clock A	770404	344
KW11-K Programmable Clock B	770432	364
AA11-K Digital- to-Analog* Converter	770416	360
DR11-K Digital I/O Interface No. 1	767770	
In	767772	310
Out	767774	324
DR11-K Digital I/O Interface No. 2	767760	

\* Digital-to-analog CSR address is at 770416 for AA11-K and I/O BUS CSR address is at 770410 for AR11. Note that the address of the digital-to-analog data buffer register, channel 0, must be specified in the device address table field of the Initialize RDA (770420 for AA11-K and 770412 for AR11).

## SENSOR I/O DEVICES

In	767762	320
Out	767764	314
DR11-K Digital I/O Interface No. 3	767750	
In	767752	330
Out	767754	334
DR11-K Digital I/O Interface No. 4	767740	
In	767742	350
Out	767744	354
DR11-K Digital I/O Interface No. 5	767730	
In	767732	370
Out	767734	374

## SPECIFICATIONS

### MECHANICAL

#### Mounting code

One hex slot in the system backplane before a UNIBUS repeater or a UNIBUS switch, one SU in the LPA11-K backplane. The first quad and hex slots in the LPA11-K backplane are used by the controller. The remaining slots are used for mounting the KW11-K clock and laboratory I/O devices. The LPA11-K backplane may be expanded as necessary for additional mounting space. NOTE: The one or two LPA11-K backplanes must mount in the same expansion box or CPU box as the hex module.



**ELECTRICAL**

Current drawn

Master microprocessor	5 A at +5 Vdc
Slave microprocessor	3 A at +5 Vdc
Interprocessor buffer	5 A at +5 Vdc, 1 A at -15 Vdc

**PERFORMANCE**

Buffer management      Multibuffered, up to eight buffers per request. Minimum size of 257 words per buffer.

Maximum channels

A/D converters	128 channels
D/A converters	4 channels
Digital I/O	5 channels
Realtime clocks	2 clocks

**ENVIRONMENTAL**

The LPA11-K conforms to the individual system's environmental specifications.

Operating temperature	41°F–122°F (5°C–50°C)
Operating relative humidity	10%–90% (non-condensing)



## CHAPTER 7

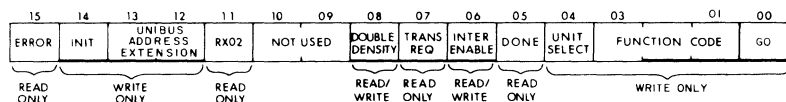
# REGISTERS

### DISK DRIVE REGISTERS

#### RX211 REGISTERS AND EXTENDED STATUS WORDS

The RX211 disk subsystems described in Chapter 2 have two registers: the Command and Status register and the Data Buffer register. The Data Buffer register is used to perform five different functions, and thus acts as five different registers. When an error is detected, a READ ERROR CODE command will cause the controller to write four extended status words into memory. These extended status words contain detailed error and status information. Following are the applicable register and extended status word diagrams and bit definitions:

#### COMMAND AND STATUS REGISTER (RX2CS) 777170



Bit	Name
-----	------

<b>15</b>	<b>ERROR</b>
-----------	--------------

When set, indicates that an error has occurred while executing a command.

The error is specified by bits in the error and status register.

Cleared by loading FUNCTION CODE <03-00> with a new command or by setting INITIALIZE <14>.

Also cleared by INIT.

<b>14</b>	<b>INITIALIZE</b>
-----------	-------------------

When set, causes the RX211 to initialize.

<b>13-12</b>	<b>UNIBUS ADDRESS EXTENSION</b>
--------------	---------------------------------

Loading these bits loads UNIBUS address bits <17,16>. Refer to the bus address register for more detail.

## DISK REGISTERS

### 11            **RX02**

This bit is set when using an RX211 subsystem and clear when using an RX11 subsystem.

### 10-09        **NOT USED**

### 08            **DOUBLE DENSITY**

When this bit is loaded with a 1, double density mode is selected.  
When this bit is loaded with a 0, single density mode is selected.

### 07            **TRANSFER REQUEST**

When set, indicates that the controller needs a word of control information.

### 06            **INTERRUPT ENABLE**

When set, allows an interrupt to occur if DONE <05> is also set.  
Cleared by loading with a 0.  
Also cleared by INIT.

### 05            **DONE**

When set, indicates that a function has been successfully executed.  
Generates an interrupt if INTERRUPT ENABLE <06> is also set.

### 04            **UNIT SELECT**

When set, selects drive 1.  
When clear, selects drive 0.

### 03-01        **FUNCTION CODE**

Loading these bits with one of the function codes listed below causes the controller to perform the corresponding operation.

01<sub>8</sub>            **FILL BUFFER**  
Causes the controller to transfer the specified number of words from memory into the internal data buffer.

03<sub>8</sub>            **EMPTY BUFFER**  
Causes the controller to transfer the specified number of words from the internal data buffer to memory.

## DISK REGISTERS

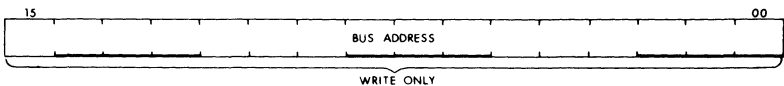
- 05<sub>8</sub>            **WRITE SECTOR**  
Causes the controller to write the contents of the internal data buffer onto the specified track and sector.
- 07<sub>8</sub>            **READ SECTOR**  
Causes the controller to read the contents of the specified track and sector and load the data into the internal data buffer.
- 11<sub>8</sub>            **SET MEDIA DENSITY**  
Causes the controller to change the density of the diskette in the selected drive and rewrite the entire diskette with zeros.
- 13<sub>8</sub>            **READ STATUS**  
Causes the controller to load the error and status register information into the data buffer register.
- 15<sub>8</sub>            **WRITE DELETED DATA SECTOR**  
Causes the controller to flag the data in the selected sector as deleted by writing a deleted data address mark.
- 17<sub>8</sub>            **READ ERROR CODE**  
Causes the controller to transfer the four extended status words into memory. The controller first requests the starting memory address by setting TRANSFER REQUEST <07>, and the processor responds by loading the bus address into the data buffer register.
- 00            **GO**

This bit resets at the end of each operation specified by FUNCTION CODE <03-01>.

### **DATA BUFFER REGISTER (RX2DB) 777172**

The data buffer register has five different functions, which cause it to act as the following five different registers at different times during program sequences.

### **BUS ADDRESS REGISTER (RX2BA)**

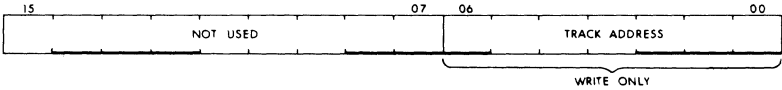


## DISK REGISTERS

This register is loaded with the starting address where data is to be read from or written into memory.

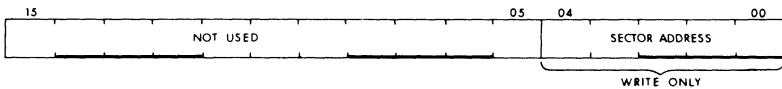
The bus address is 18 bits. The low-order 16 bits are loaded by this register and the high-order two bits are loaded by ADDRESS EXTENSION <13,12> in the command and status register.

### TRACK ADDRESS REGISTER (RX2TA)



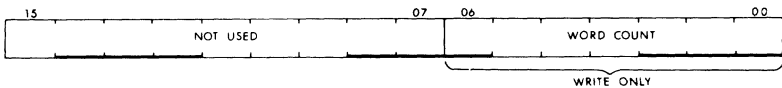
This register specifies the diskette track (0-76<sub>10</sub>) on which the operation is to be performed.

### SECTOR ADDRESS REGISTER (RX2SA)



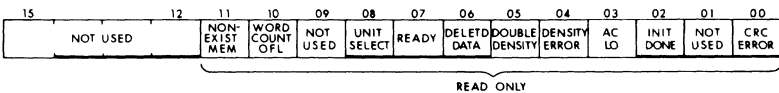
This register specifies the diskette sector (1-26<sub>10</sub>) in which the operation is to be performed.

### WORD COUNT REGISTER (RX2WC)



This register specifies the number of data words (128<sub>10</sub> in double density mode and 64<sub>10</sub> in single density mode) to be transferred.

### ERROR AND STATUS REGISTER (RX2ES)



This register is loaded with error and status information at the completion of each operation.

## DISK REGISTERS

Bit	Name
-----	------

---

15-12	<b>NOT USED</b>
-------	-----------------

11	<b>NON-EXISTENT MEMORY</b>
----	----------------------------

Set when the controller attempts to transfer data into or from a memory address which does not exist.

10	<b>WORD COUNT OVERFLOW</b>
----	----------------------------

When set, indicates that the specified word count is larger than  $128_{10}$  ( $64_{10}$  in single density mode).

09	<b>NOT USED</b>
----	-----------------

08	<b>UNIT SELECT</b>
----	--------------------

When set, indicates that drive 1 has been selected.  
When clear, indicates that drive 0 has been selected.

07	<b>READY</b>
----	--------------

When set, indicates that the selected drive has a diskette loaded and is ready to perform an operation.

06	<b>DELETED DATA</b>
----	---------------------

When set, indicates that the data in the sector specified by the READ SECTOR command has been deleted.

05	<b>DOUBLE DENSITY</b>
----	-----------------------

When set, indicates that the diskette on the selected drive is written in double density mode.

04	<b>DENSITY ERROR</b>
----	----------------------

When set, indicates that the density of the diskette does not match the density mode of the selected drive.

03	<b>AC LO</b>
----	--------------

When set, indicates that the RX02 floppy disk drives have lost AC power.

02	<b>INITIALIZE DONE</b>
----	------------------------

When set, indicates that the RX211 has been initialized.

## DISK REGISTERS

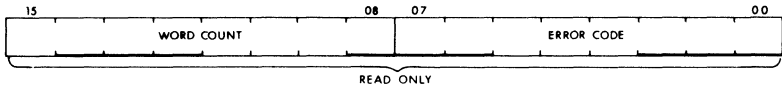
Set by INITIALIZE <14> in the command and status register, by turning on the RX02s, or by INIT.

**01 NOT USED**

**00 CRC ERROR**

When set, indicates that a data error has been detected.

### EXTENDED STATUS WORD 1



**Bit Name**

---

**15-08 WORD COUNT**

These bits contain the word count used during the last operation.

**07-00 ERROR CODE**

These bits are loaded with one of the following error codes:

010<sub>8</sub> Drive 0 failed to see home on initialize.

020<sub>8</sub> Drive 1 failed to see home on initialize.

040<sub>8</sub> The processor loaded the track address register with a number greater than 76<sub>10</sub>.

050<sub>8</sub> Home was found before the desired track was reached.

070<sub>8</sub> The microprocessor controller did not find the desired sector after looking at 52 headers (2 revolutions).

110<sub>8</sub> The microprocessor controller found not SEP clock after 40 $\mu$ s.

120<sub>8</sub> Preamble not found.

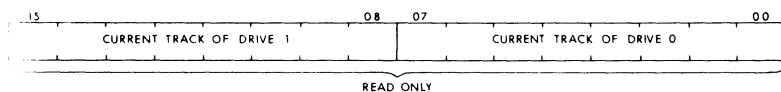
130<sub>8</sub> Preamble found but no ID burst found within allowable time span.



## DISK REGISTERS

- 150<sub>8</sub>            The track reached does not match the header track address.
  
- 160<sub>8</sub>            The microprocessor controller made too many attempts for an IDAM (identifies header).
  
- 170<sub>8</sub>            Data AM not found within allowable time span.
  
- 200<sub>8</sub>            CRC error detected while reading the sector from the disk. No code appears in the error register.
  
- 220<sub>8</sub>            Read/write electronics failed Maintenance mode test.
  
- 230<sub>8</sub>            Word count overflow.
  
- 240<sub>8</sub>            Density error.
  
- 250<sub>8</sub>            Wrong key word for Set Media Density command.

### EXTENDED STATUS WORD 2



Bit	Name
-----	------

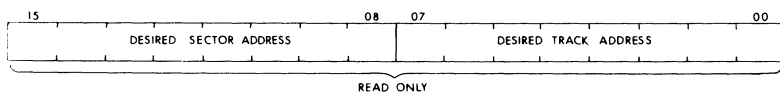
<b>15-08</b>	<b>CURRENT TRACK OF DRIVE 1</b>
--------------	---------------------------------

These bits contain the address of the track at which drive 1's head is positioned.

<b>07-00</b>	<b>CURRENT TRACK OF DRIVE 0</b>
--------------	---------------------------------

These bits contain the address of the track at which drive 0's head is positioned.

### EXTENDED STATUS WORD 3



## DISK REGISTERS

**Bit            Name**

---

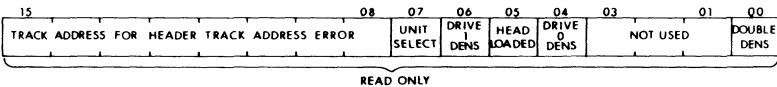
**15-08            DESIRED SECTOR ADDRESS**

These bits contain the sector address specified by the last operation.

**07-00            DESIRED TRACK ADDRESS**

These bits contain the track address specified by the last operation.

**EXTENDED STATUS WORD 4**



**Bit            Name**

---

**15-08            TRACK ADDRESS FOR HEADER TRACK ADDRESS ERROR**

These bits contain the track address when the error code in the extended status word 1 equals 150<sub>8</sub>.

**07                UNIT SELECT**

When set, indicates that drive 1 is selected.  
When clear, indicates that drive 0 is selected.

**06                DRIVE 1 DENSITY**

When set, indicates that drive 1 is in double density mode.  
When clear, indicates that drive 1 is in single density mode.

**05                HEAD LOADED**

When set, indicates that the head of the selected drive is in contact with the diskette.

**04                DRIVE 0 DENSITY**

When set, indicates that drive 0 is in double density mode.  
When clear, indicates that drive 0 is in single density mode.

**03-01            NOT USED**

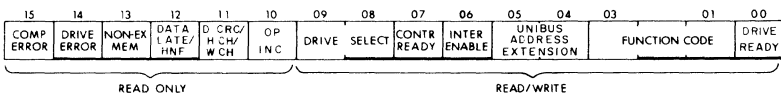
**00                DOUBLE DENSITY**

When set, indicates that the diskette on the selected drive is written in double density mode.

## RL01/RL02 REGISTERS

The RL11 and RL211 subsystems described in Chapter 2 use the same controller. The controller has four registers: the Control and Status Register, the Bus Address Register, the Disk Address Register, and the Multipurpose Register. Following are the applicable register drawings and bit definitions. These register diagrams and bit definitions refer to both PDP-11 and VAX configurations, unless noted. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the UNIBUS adapter registers.

### CONTROL AND STATUS REGISTER (RLCS) 774400



Bit	Name
-----	------

<b>15</b>	<b>COMPOSITE ERROR</b>
-----------	------------------------

When set, indicates that one or more of bits <14-10> is set. Generates an interrupt if INTERRUPT ENABLE <06> is also set.

<b>14</b>	<b>DRIVE ERROR</b>
-----------	--------------------

When set, indicates that the selected drive has detected an error. Additional status information can be obtained by executing a GET STATUS command and then reading the multipurpose register.

<b>13</b>	<b>NON-EXISTENT MEMORY</b>
-----------	----------------------------

When set, indicates that the controller attempted to transfer data to or from a memory address specified by the bus address register which does not exist.

<b>12</b>	<b>DATA LATE or HEADER NOT FOUND</b>
-----------	--------------------------------------

When set and OPERATION INCOMPLETE <10> is also set, indicates that the correct sector header was not yet found after 200 ms.

When set and OPERATION INCOMPLETE <10> is not set, indicates that the controller was unable to supply a data word during a WRITE operation or accept a data word during a READ operation at the time that the drive requested a transfer.

**11 DATA CRC or HEADER CHECK or WRITE CHECK**

When set and OPERATION INCOMPLETE <10> is also set, indicates that a header check error has been detected.

When set, and OPERATION INCOMPLETE <10> is not set during a READ operation, indicates that a data error has been detected (DATA CRC).

When set, and OPERATION INCOMPLETE <10> is not set during a WRITE CHECK operation, indicates that the data on the disk did not match the data in memory.

**10 OPERATION INCOMPLETE**

When set and bits <11-12> are clear, indicates that the current operation was not yet completed after 200 ms.

**09-08 DRIVE SELECT**

These bits select drives 0-3.

**07 CONTROLLER READY**

When set, indicates that the controller is ready to accept a command.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

When loaded with a 0 causes the controller to execute the command in FUNCTION CODE <03-01>.

**06 INTERRUPT ENABLE**

When set, generates an interrupt if CONTROLLER READY <07> or DRIVE READY <00> is also set.

**05-04 UNIBUS ADDRESS EXTENSION**

Loading these bits loads UNIBUS address bits <17, 16>. Refer to the bus address register for more detail.

**03-01 FUNCTION CODE**

These bits specify the following operations to be performed by the selected drive. CONTROLLER READY <07> must be loaded with a 1 to cause the drive to execute the command.

5<sub>8</sub> WRITE DATA

1<sub>8</sub> WRITE CHECK DATA

6<sub>8</sub> READ DATA

## DISK REGISTERS

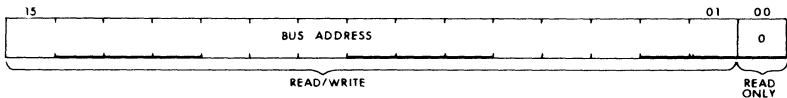
4 <sub>8</sub>	READ HEADER
7 <sub>8</sub>	READ DATA WITHOUT HEADER CHECK
3 <sub>8</sub>	SEEK
2 <sub>8</sub>	GET STATUS
0 <sub>8</sub>	NO OPERATION

### 00 DRIVE READY

When set, indicates that the selected drive is ready to accept a command.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

### BUS ADDRESS REGISTER (RLBA) 774402



Bit	Name
-----	------

### 15-01 BUS ADDRESS

This register is loaded with the starting address where data is to be written from or read into memory .

The bus address is 18 bits. The low-order 16 bits are loaded by the bus address register and the high-order 2 bits are loaded by bits <05-04> in the control and status register. During READ and WRITE operations the bus address is incremented by two for each word transferred to or from memory.

### 00 BUS ADDRESS

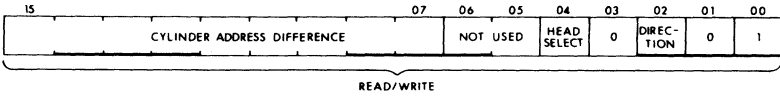
This bit is always 0.

### DISK ADDRESS REGISTER (RLDA) 774404

The disk address register is loaded with control information before each of the following operations: SEEK, READ or WRITE, and GET STATUS. The register diagrams and bit definitions for each of the operations are as follows:

## DISK REGISTERS

### DISK ADDRESS REGISTER DURING A SEEK OPERATION



**Bit**            **Name**

---

**15-07**            **CYLINDER ADDRESS DIFFERENCE**

These bits specify the number of cylinders the drive is to move the heads during a SEEK operation.

**06-05**            **NOT USED**

**04**                **HEAD SELECT**

These bits specify which head is to be used (track select).

**03**

This bit is always 0.

**02**                **DIRECTION**

When set, causes the drive to move the heads toward the spindle during a SEEK operation (higher cylinder addresses).

When clear, causes the drive to move the heads away from the spindle during a SEEK operation (lower cylinder addresses).

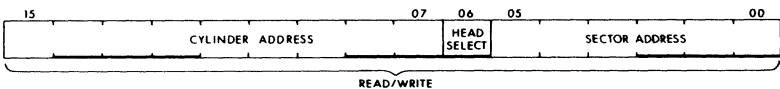
**01**

This bit is always 0.

**00**

This bit is always 1.

### DISK ADDRESS REGISTER DURING A READ OR WRITE OPERATION



## DISK REGISTERS

**Bit            Name**

---

**15-07        CYLINDER ADDRESS**

These bits specify the cylinder address (0-511<sub>10</sub> for the RL02, 0-255<sub>10</sub> for the RL01) of the desired sector.

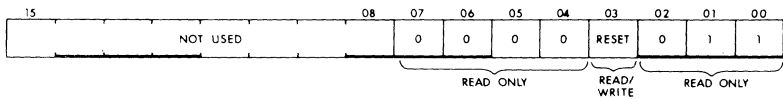
**06            HEAD SELECT**

These bits specify which head is to be used (track select).

**05-00        SECTOR ADDRESS**

These bits specify the sector address (0-39<sub>10</sub>) of the desired sector.

### DISK ADDRESS REGISTER DURING A GET STATUS OPERATION



**Bit            Name**

---

**15-08        NOT USED**

**07-04**

These bits are always 0.

**03            RESET**

When set, causes the drive to clear its error register before sending a status word to the controller.

**02**

This bit is always 0.

**01-00**

These bits are always 1.

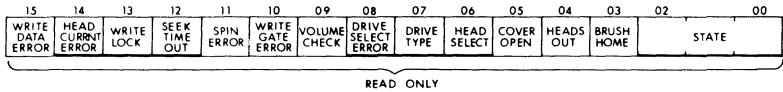
### MULTIPURPOSE REGISTER (RPCS2) 774406

The multipurpose register is loaded with control information before a READ or WRITE operation. It also provides additional status information after a GET STATUS operation and contains the header field data

## DISK REGISTERS

after a READ HEADER operation. The register diagrams and bit definitions for each of the operations are as follows:

### MULTIPURPOSE REGISTER AFTER A GET STATUS OPERATION



Bit	Name
-----	------

<b>15</b>	<b>WRITE DATA ERROR</b>
-----------	-------------------------

When set, indicates that no transitions were detected on the write data line when Write Gate was asserted.

<b>14</b>	<b>HEAD CURRENT ERROR</b>
-----------	---------------------------

When set, indicates that write current has been detected in the heads when Write Gate was not asserted.

<b>13</b>	<b>WRITE LOCK</b>
-----------	-------------------

When set, indicates that the selected drive is write-protected (write protect switch on front panel is set).

<b>12</b>	<b>SEEK TIME OUT</b>
-----------	----------------------

When set, indicates that the drive did not completed a SEEK operation within the allowable time span.

<b>11</b>	<b>SPIN ERROR</b>
-----------	-------------------

When set, indicates that the disk spindle is spinning too fast or too slowly.

<b>10</b>	<b>WRITE GATE ERROR</b>
-----------	-------------------------

When set, indicates that Write Gate is asserted and 1) the drive is not "ready to read/write", 2) the drive is write-protected, 3) Sector Pulse is occurring, or 4) the drive has another error.

<b>09</b>	<b>VOLUME CHECK</b>
-----------	---------------------

When set, indicates that a disk cartridge has been mounted and the disk is up to speed.

Cleared by executing a GET STATUS command when RESET <03> in the disk address register is set.



## DISK REGISTERS

### **08 DRIVE SELECT ERROR**

When set, indicates that more than one drive has been selected.

### **07 DRIVE TYPE**

When set, indicates that the drive selected is an RL02.

When clear, indicates that the drive selected is an RL01.

### **06 HEAD SELECT**

This bit indicates which head has been selected.

### **05 COVER OPEN**

When set, indicates that the drive access cover is open or the dust cover is not in place.

### **04 HEADS OUT**

When set, indicates that the heads are on the disk.

### **03 BRUSH HOME**

When set, indicates that the brushes are retracted and not over the disk.

### **02-00 STATE**

These bits indicate the status of the drive.

$0_8$  LOAD CARTRIDGE

$1_8$  SPIN UP

$2_8$  BRUSH CYCLE

$3_8$  LOAD HEADS

$4_8$  SEEK

$5_8$  LOCK ON

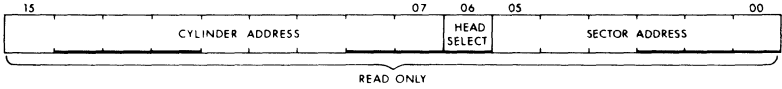
$6_8$  UNLOAD HEADS

$7_8$  SPIN DOWN

## DISK REGISTERS

### MULTIPURPOSE REGISTER AFTER A READ HEADER OPERATION

After a READ HEADER operation, the multipurpose register provides header field data from the specified sector. The header field data is contained in three words, which are read sequentially from the multipurpose register. The diagrams and bit definitions of these three words are as follows:



Bit	Name
-----	------

15-07	CYLINDER ADDRESS
-------	------------------

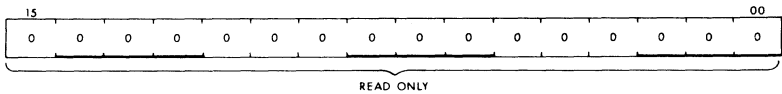
These bits contain the cylinder address read from the sector header.

06	HEAD SELECT
----	-------------

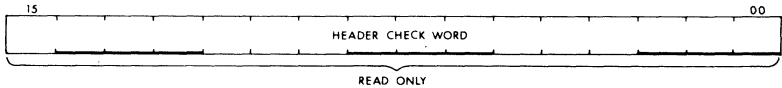
This bit contains the head select (track address) read from the sector header.

05-00	SECTOR ADDRESS
-------	----------------

These bits contain the sector address read from the sector header.

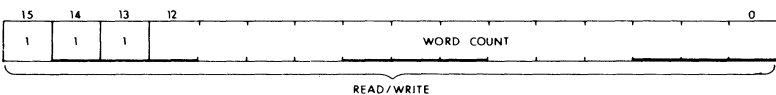


This register contains all zeros.



This register contains the header CRC.

### MULTIPURPOSE REGISTER DURING A READ OR WRITE OPERATION



## DISK REGISTERS

**Bit**            **Name**

---

**15-13**

These bits are always 1.

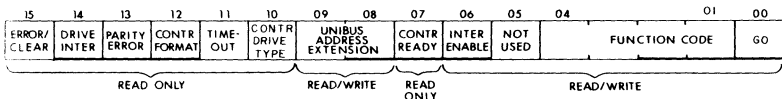
**12-00**            **WORD COUNT**

These bits must be loaded with the two's complement of the number of words (1-5120<sub>10</sub>) to be transferred during a READ or WRITE operation. Successive sectors can be read or written, but only up to the end of the current track. A SEEK command must be issued to change heads (tracks) or cylinders.

### RK07 REGISTERS

The RK711 subsystems described in Chapter 2 have 16 registers. Following are the applicable register drawings and bit definitions. These register diagrams and bit definitions refer to both PDP-11 and VAX configurations, unless noted. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the UNIBUS adapter registers.

#### CONTROL AND STATUS 1 REGISTER (RKCS1) 777440



**Bit**            **Name**

---

**15**            **COMBINED ERROR/CONTROLLER CLEAR**

When set, indicates that one or more of the error bits in this register, the control and status 2 register, or the error register is set.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

When loaded with a 1, clears error bits in the controller and initializes the controller but does not affect the drives.

**14**            **DRIVE INTERRUPT**

When set, indicates that one or more of the ATTENTION bits <07-00> in the attention summary register are set.

## DISK REGISTERS

### 13 DRIVE TO CONTROLLER PARITY ERROR

When set, indicates that the controller detected a data parity error during a READ operation.

### 12 CONTROLLER FORMAT

When set, the controller uses 18-bit word format.

When clear, the controller uses normal 16-bit word format (this bit should always be clear).

### 11 CONTROLLER TIME-OUT

When set, indicates that the GO <00> bit has been set for more than 800 ms and that the operation has not yet been completed.

### 10 CONTROLLER DRIVE TYPE

When set, indicates that the controller is configured to connect to RK07 disk drives.

When clear, indicates that the controller is configured to connect to RK06 disk drives.

### 09-08 UNIBUS ADDRESS EXTENSION

Loading these bits loads UNIBUS address bits <17, 16>.

Refer to the description of the bus address register for more detail.

### 07 CONTROLLER READY

When set, indicates that the controller is ready to accept a command.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

### 06 INTERRUPT ENABLE (PDP-11 only)

When set, generates an interrupt if CONTROLLER READY <07>, DRIVE INTERRUPT <14>, or COMBINED ERROR <15> is also set.

### 05 NOT USED

### 04-01 FUNCTION CODE

Loading these bits with one of the function codes listed below causes the selected drive to perform the corresponding operation.

01<sub>8</sub> SELECT DRIVE

23<sub>8</sub> WRITE DATA

31<sub>8</sub> WRITE CHECK





## DISK REGISTERS

**Bit**            **Name**

---

**15**            **DATA LATE**

Set when the controller is unable to supply a data word during a WRITE operation or accept a data word during a READ operation at the time that the drive requests a transfer.

**14**            **WRITE CHECK ERROR**

Set when the controller is performing a WRITE CHECK operation and a word on the disk does not match the corresponding word in memory.

**13**            **UNIBUS PARITY ERROR**

Set if a UNIBUS data parity error is detected during a WRITE operation.

**12**            **NON-EXISTENT DRIVE**

Set when the processor's attempt to load a register fails because the drive selected by DRIVE SELECT <02-00> does not exist or is turned off.

**11**            **NON-EXISTENT MEMORY**

Set when the controller attempts to transfer data into or from a memory address specified by the bus address register which does not exist. The bus address register will contain the address +2 of the memory location that does not exist.

**10**            **PROGRAM ERROR**

Set when the program attempts to load a new command into FUNCTION CODE <04-01> in the control and status 1 register when CONTROLLER READY <07> in the control and status 1 register is not set, i.e. when the controller is not ready to accept a command. The new command will not be loaded.

**09**            **MULTIPLE DRIVE SELECT**

When set, indicates that more than one drive has been selected at the same time.

**08**            **UNIT FIELD ERROR**

When set, indicates that more than one drive has been selected.

## DISK REGISTERS

### 07 OUTPUT READY

This bit is used only for testing the controller.

When set, indicates that the data buffer register contains a word and may be read.

### 06 INPUT READY

This bit is used only for testing the controller.

When set, indicates that the data buffer register is not full and may be loaded.

### 05 SUBSYSTEM CLEAR

When set, clears all error bits and initializes the controller and all of the drives.

### 04 BUS ADDRESS INCREMENT INHIBIT

When set, prevents the controller from incrementing the bus address register during a data transfer. Therefore, all data words are read from or written into the same memory location.

### 03 RELEASE

This bit is used for dual-access drives.

When set, deselects the drive to allow it to be selected by the other controller.

### 02-00 DRIVE SELECT

These bits are loaded to select the disk drive (0-7). This address is set by the numbered address plug in the drive.

## DRIVE STATUS REGISTER (RKDS) 777452

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
STATUS VALID	CURR DRIVE ATTN	POS IN PROG	NOT USED	WRITE LOCK	NOT USED	DISK DRIVE TYPE	DRIVE READY	VOLUME VALID	DRIVE OFF TRACK	SPEED LOSS	DRIVE AC LO	OFFSET	NOT USED	DRIVE AVAIL	

READ ONLY

**Bit**                      **Name**

---

### 15 STATUS VALID

When set, indicates that the bits in the drive status register and the error register have been updated.



## DISK REGISTERS

### 14            **CURRENT DRIVE ATTENTION**

When set, indicates that one of the drives that is not currently selected has a status change to report.

### 13            **POSITIONING IN PROGRESS**

Set when the selected drive is performing a positioning operation.

### 12            **NOT USED**

### 11            **WRITE LOCK**

When set, indicates that the selected drive is write-protected (write protect switch on front panel is set).

### 10-09       **NOT USED**

### 08            **DISK DRIVE TYPE**

When set, indicates that the selected drive is an RK07.  
When clear, indicates that the selected drive is an RK06.

### 07            **DRIVE READY**

Set when the selected drive is ready to execute a command.

### 06            **VOLUME VALID**

When clear, indicates that the drive has been put off-line and then on-line and that the disk cartridge may have been changed.  
Cleared by the drive coming on-line.  
Set by PACK ACKNOWLEDGE command.

### 05            **DRIVE OFF TRACK**

When set, indicates that the drive was not centered on the track during a WRITE operation.

### 04            **SPEED LOSS**

When set, indicates that the disk cartridge is spinning too slowly.

### 03            **DRIVE AC LO**

When set, indicates that the AC power in the selected drive has failed.

### 02            **OFFSET**

When set, indicates that the selected drive is in Offset mode.

## DISK REGISTERS

**01            NOT USED**

**00            DRIVE AVAILABLE**

When set, indicates that the selected drive is available and not being used by the other controller in a dual-access system.

### ERROR REGISTER (RKER) 777454

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	DRIVE UNSAFE	OP INC	DRIVE TIMING ERROR	WRITE LOCK ERROR	INVLD ADDR	ADDR OVER- FLOW	HEADER CHECK ERROR	BAD SECTOR ERROR	ECC HARD ERROR	DRIVE TYPE ERROR	FORMAT ERROR	PARITY ERROR	NON-EX FUNC	SEEK INC	ILL FUNC

READ ONLY

**Bit            Name**

**15            DATA CHECK**

When set, indicates a data error has been detected during a READ operation, i.e. that the ECC generated does not match the ECC read from the sector.

**14            DRIVE UNSAFE**

When set, indicates that the drive has detected a hardware fault and unloaded the heads.

**13            OPERATION INCOMPLETE**

When set, indicates that the drive positioned the heads to the desired cylinder but was not able to find the specified sector.

**12            DRIVE TIMING ERROR**

Set when a failure has been detected in the clocking or timing circuits of the drive.

**11            WRITE LOCK ERROR**

When set, indicates that the processor attempted to write on a write-protected drive (write protect switch on front panel switch is set).

**10            INVALID ADDRESS**

When set, indicates that the sector address specified by the desired cylinder register and the disk address registers is invalid.

## DISK REGISTERS

### 09 ADDRESS OVERFLOW

When set, indicates that the desired cylinder register has reached a count of more than 814.

### 08 HEADER CHECK ERROR

When set, indicates that the header check word generated does not match the header check word read from the sector.

### 07 BAD SECTOR ERROR

When set, the sector header field indicates that the sector is bad.

### 06 ECC HARD ERROR

When set, indicates that the data error cannot be corrected by the Error Correction Code (ECC) circuitry.

### 05 DRIVE TYPE ERROR

When set, indicates that the controller is not configured (RK06 or RK07) to match the drive, i.e. CONTROLLER DRIVE TYPE <10> in the control and status 1 register does not match DISK DRIVE TYPE <08> in the drive status register.

### 04 FORMAT ERROR

When set, indicates that the format (16-bit or 18-bit) of the disk cartridge does not match the format of the controller.

The format of the controller is set by loading CONTROLLER FORMAT <12> in the control and status 1 register and the format of the cartridge is written into the header field when the cartridge is formatted.

### 03 CONTROLLER TO DRIVE PARITY ERROR

When set, indicates that the drive has detected a data parity error in the information received from the controller.

### 02 NON-EXECUTABLE FUNCTION

When set, indicates that a SEEK or DATA TRANSFER operation was attempted while VOLUME VALID <06> in the drive status register was clear.

### 01 SEEK INCOMPLETE

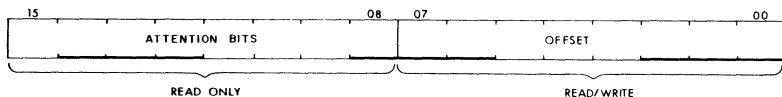
When set, indicates that a SEEK operation has failed.

# DISK REGISTERS

## 00 ILLEGAL FUNCTION

When set, indicates that an invalid function code has been loaded into FUNCTION CODE <04-01> in the control and status 1 register.

## ATTENTION SUMMARY/OFFSET REGISTER (RKAS/OF) 777456



**Bit Name**

---

### 15-08 ATTENTION BITS

These bits <15-08> are the attention interrupt lines for disk drives 7-0.

### 07-00 OFFSET

These bits specify the direction and amount to shift the heads off the center of the track during an OFFSET operation.

## DESIRED CYLINDER REGISTER (RKDC) 777460



**Bit Name**

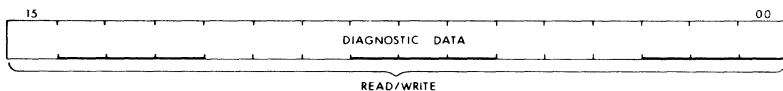
---

### 15-10 NOT USED

### 09-00 DESIRED CYLINDER ADDRESS

These bits select the cylinder address (0-814<sub>10</sub>) at which the heads are to be positioned.

## DATA BUFFER REGISTER (RKDB) 777464







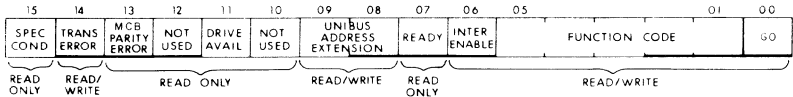
## DISK REGISTERS

signed according to the unit plug on the device. The range of byte offset bases for each of the up to eight devices supported by an MBA are as follows: 400, 480, 500, 580, 600, 680, 700, and 780. The VAX byte offsets shown here are relative to the base of the device registers.

### CONTROL AND STATUS 1 REGISTER (CS1)

**776700 (PDP-11)**

**BYTE OFFSET=0 (VAX)**



**Bit            Name**

#### 15            SPECIAL CONDITION (PDP-11 ONLY)

Set by TRANSFER ERROR <14> or MASSBUS CONTROL BUS PARITY ERROR <13> in the control and status 1 register, or ATTENTION <15> in any of the drive status registers.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

Cleared by resetting the error bit that caused SPECIAL CONDITION to set.

#### 14            TRANSFER ERROR (PDP-11 only)

Set by any of the following bits in the control and status 2 register: DATA LATE <15>, WRITE CHECK ERROR <14>, PARITY ERROR <13>, NON-EXISTENT DRIVE <12>, NON-EXISTENT MEMORY <11>, PROGRAM ERROR <10>, MISSED TRANSFER <09>, or MASSBUS DATA PARITY ERROR <08>.

Sets SPECIAL CONDITION <15>.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or by loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

#### 13            MASSBUS CONTROL BUS PARITY ERROR (PDP-11 ONLY)

Set when a parity error is detected while reading a drive register. A parity error detected while writing a drive register sets MASSBUS CONTROL BUS PARITY ERROR <03> in the error 1 register.

Sets SPECIAL CONDITION <15>.

## DISK REGISTERS

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or by loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by INIT.

**12**            **NOT USED**

**11**            **DRIVE AVAILABLE (PDP-11 only)**

When set, indicates that the selected drive is present, turned on, and not being used by the other MASSBUS port.

**10**            **NOT USED**

**09-08**        **UNIBUS ADDRESS EXTENSION (PDP-11 only)**

Loading these bits loads UNIBUS address bits <17, 16>. In the PDP-11/70 these bits can also be loaded by the bus address extension register.

Refer to the bus address register for more detail.

Cleared by loading with zeros.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**07**            **READY (PDP-11 only)**

When set, indicates that the controller is ready to accept a command. Generates an interrupt when the READY bit is set if INTERRUPT ENABLE <06> is also set.

Cleared while the controller is executing a command.

**06**            **INTERRUPT ENABLE (PDP-11 only)**

When set, generates an interrupt if READY <07> or SPECIAL CONDITION <15> is also set.

In the PDP-11/70 this bit is the same as INTERRUPT ENABLE <06> in the control and status 3 register.

Cleared when the interrupt is serviced by the processor.

Also cleared by INIT.

**05-01**        **FUNCTION CODE**

Loading these bits with one of the function codes listed below causes the selected drive to perform the corresponding operation.

**61<sub>8</sub>**            **WRITE DATA**

**51<sub>8</sub>**            **WRITE CHECK DATA**

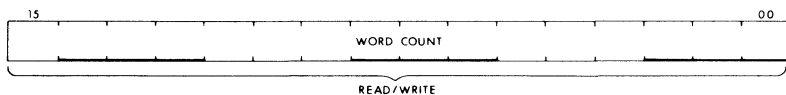


## DISK REGISTERS

63 <sub>8</sub>	WRITE HEADER AND DATA
53 <sub>8</sub>	WRITE CHECK HEADER AND DATA
71 <sub>8</sub>	READ DATA
73 <sub>8</sub>	READ HEADER AND DATA
05 <sub>8</sub>	SEEK
07 <sub>8</sub>	RECALIBRATE
17 <sub>8</sub>	RETURN TO CENTERLINE
15 <sub>8</sub>	OFFSET
31 <sub>8</sub>	SEARCH
13 <sub>8</sub>	RELEASE MASSBUS PORT
21 <sub>8</sub>	READ-IN PRESET
23 <sub>8</sub>	PACK ACKNOWLEDGE
11 <sub>8</sub>	DRIVE CLEAR
01 <sub>8</sub>	NO OPERATION
00	GO

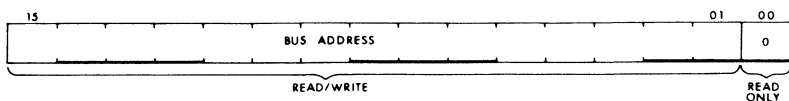
This bit resets at the end of each operation specified by FUNCTION CODE <05-01>.

### WORD COUNT REGISTER (WC) 776702 (PDP-11 ONLY)



This register is loaded with the two's complement of the number of data words to be transferred to or from memory.

### BUS ADDRESS REGISTER (BA) 776704 (PDP-11 ONLY)



## DISK REGISTERS

**Bit**            **Name**

---

**15-01**            **BUS ADDRESS**

This register is loaded with the starting address where data is to be written from or read into memory.

For PDP-11 systems, except the PDP-11/70, the bus address is 18 bits. The low-order 16 bits are loaded by the bus address register and the high-order 2 bits are loaded by bits <09-08> in the control and status 1 register. During READ and WRITE operations the bus address is incremented by two for each word transferred to or from memory.

For PDP-11/70 systems only, the bus address is 22 bits. The low-order 16 bits are loaded by the bus address register and the high-order 6 bits are loaded by bits <05-01> in the bus address extension register. The PDP-11/70 uses double word transfers, i.e. two words at a time. During READ and WRITE operations the bus address is incremented by four for each double word transferred to or from memory.

Cleared by loading with zeros.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

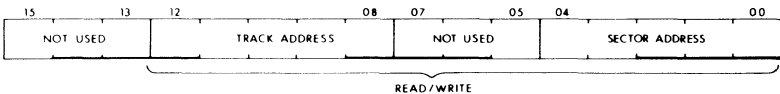
**00**                **BUS ADDRESS**

This bit is always 0.

### DESIRED SECTOR/TRACK ADDRESS REGISTER (DA)

**776706 (PDP-11)**

**Byte Offset=14 (VAX)**



**Bit**            **Name**

---

**15-13**            **NOT USED**

**12-08**            **TRACK ADDRESS**

These bits are loaded with a number (0-13<sub>10</sub> for the RM80, 0-18<sub>10</sub> for the RM05, and 0-4<sub>10</sub> for the RM02/03) which specifies the track on which the data transfer is to start.

The number is incremented by the drive at the end of the last sector of a track.

## DISK REGISTERS

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by INIT.

**07-05        NOT USED**

**04-00        SECTOR ADDRESS**

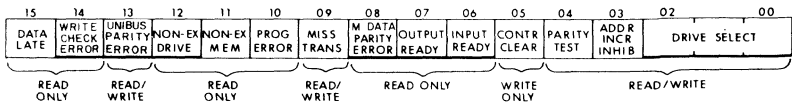
These bits are loaded with a number (0-31<sub>10</sub>) which specifies the sector at which the data transfer is to start.

The number is incremented by the drive after each sector has been transferred.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### CONTROL AND STATUS 2 REGISTER (CS2) 776710 (PDP-11 ONLY)



Bit	Name
-----	------

<b>15</b>	<b>DATA LATE</b>
-----------	------------------

Set when the controller is unable to supply a data word during a WRITE operation or accept a data word during a READ operation at the time that the drive requests a transfer.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

<b>14</b>	<b>WRITE CHECK ERROR</b>
-----------	--------------------------

Set when the controller is performing a WRITE CHECK operation and a word on the disk does not match the corresponding word in memory.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

## DISK REGISTERS

Also cleared by INIT.

### 13 UNIBUS PARITY ERROR

Set if a UNIBUS data parity error is detected during a WRITE operation. The bus address register will contain the address +2 (address +4 for PDP-11/70 systems) of the memory word with the parity error unless BUS ADDRESS INCREMENT INHIBIT <03> is not set.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 12 NON-EXISTENT DRIVE

Set when a READ or WRITE operation attempt fails because the drive selected by DRIVE SELECT <02-00> does not exist or is turned off.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 11 NON-EXISTENT MEMORY

Set when the controller attempts to transfer data into or from a memory address specified by the bus address register which does not exist. The bus address register will contain the address +2 (address +4 for PDP-11/70 systems) of the memory location that does not exist.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 10 PROGRAM ERROR

Set when the program attempts to load a new command into FUNCTION CODE <05-01> in the control and status 1 register when READY <07> in the control and status 1 register is not set, i.e. when the controller is not ready to accept a command. The new command will not be loaded.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**09 MISSED TRANSFER**

Set if the drive does not respond to a DATA TRANSFER command, usually because ERROR SUMMARY <14> in the drive status register is set.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**08 MASSBUS DATA PARITY ERROR**

Set when a MASSBUS data parity error is detected during a READ operation. A parity error detected during a WRITE operation sets PARITY ERROR <03> in the error 1 register.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-00> in the control and status 1 register.

Also cleared by INIT.

**07 OUTPUT READY**

This bit is used only for testing the controller.

When set, indicates that the data buffer register contains a word and may be read.

Cleared by reading the data buffer register or setting CONTROLLER CLEAR <05>.

Also cleared by INIT.

**06 INPUT READY**

This bit is used only for testing the controller.

When set, indicates that the data buffer register is not full and may be loaded.

Cleared when the data buffer is fully loaded.

**05 CONTROLLER CLEAR**

When set, clears all error bits and initializes the controller and all of the drives.

**04 PARITY TEST**

When set, causes the controller to generate and check for even parity

## DISK REGISTERS

on the MASSBUS control bus and to generate even parity but check for odd parity on the MASSBUS data bus.

When clear, the controller generates and checks for odd parity on both the MASSBUS control bus and the MASSBUS data bus.

Cleared by loading with a 0.

Also cleared by setting CONTROLLER CLEAR <05> or INIT.

### 03 UNIBUS MEMORY ADDRESS INCREMENT INHIBIT

When set, prevents the controller from incrementing the bus address register during a data transfer. Therefore, all data words are read from or written into the same memory location.

Cleared by loading with a 0.

Also cleared by setting CONTROLLER CLEAR <05> or INIT.

### 02-00 DRIVE SELECT

These bits are loaded to select the disk drive (0-7). This address is set by the numbered address plug in the drive.

## DRIVE STATUS REGISTER (DS)

776712 (PDP-11)

BYTE OFFSET = 4 (VAX)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATTN	ERROR SUM	POS IN PROG	MED ON-LINE	WRITE LOCK	LAST SECTOR TRANS	DUAL- ACCESS ENABLD	DRIVE PRES	DRIVE READY	VOLUME VALID	DIFF EQ 1	DIFF LESS TH 64	GO REV	GUARD BAND	20 IN/S	5 IN/S
READ ONLY															

<b>Bit</b>	<b>Name</b>
------------	-------------

### 15 ATTENTION (ATTN, ATA)

When set, indicates that an error or some unusual condition exists in the drive.

Sets SPECIAL CONDITION <15> in the control and status 1 register.

Cleared by loading any command into FUNCTION CODE <05-00> in the control and status 1 register if ERROR SUMMARY <14> is not set.

Cleared by loading the DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or by loading a 1 into the appropriate bit position in the attention summary register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 14 ERROR SUMMARY

Set by any bit in the error 1 or error 2 registers.

## DISK REGISTERS

When set, the drive will accept no commands other than DRIVE CLEAR.

Sets ATTENTION <15>.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or setting CONTROLLER CLEAR <05> in the control and status 2 register.

Also cleared by INIT.

### 13            **POSITIONING IN PROGRESS**

Set when the selected drive is performing a positioning operation (SEEK, OFFSET, RETURN TO CENTERLINE, RECALIBRATE, UNLOAD, and SEARCH).

Cleared at the end of the operation.

### 12            **MEDIUM ON-LINE**

Set when the selected drive has a disk pack mounted, is on-line, and ready to execute a command.

A change in the state of MEDIUM ON-LINE sets ATTENTION <15> and generates an interrupt.

### 11            **WRITE LOCK**

When set, indicates that the selected drive is write-protected (the write protect switch on the front panel is set).

### 10            **LAST SECTOR TRANSFERRED**

When set, indicates that cylinder 822, track 18, sector 31 (the last addressable sector) has been read or written.

### 09            **DUAL-ACCESS ENABLED (PROGRAMMABLE)**

When set, indicates that the port select switch on the selected drive is in the A/B position and that the drive is available to both MASSBUS ports.

### 08            **DRIVE PRESENT**

When set, indicates that the selected drive is turned on.

### 07            **DRIVE READY**

Set when the selected drive is ready to execute a command.

### 06            **VOLUME VALID**

When clear, indicates that the drive has been put off-line and then on-

## DISK REGISTERS

line and that the disk pack may have been changed.

Cleared by the drive coming on-line.

Set by PACK ACKNOWLEDGE or READ-IN PRESET command.

**05-01      NOT USED**

**00            OFFSET MODE**

When set, indicates that the drive is in Offset mode.

Refer to the description of OFFSET DIRECTION <07> in the offset register for more detail.

### ERROR 1 REGISTER (ER1)

**776714 (PDP-11)**

**BYTE OFFSET = 8 (VAX)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	UNSAFE	OP INC	DRIVE TIMING ERROR	WRITE LOCK ERROR	INVLD ADDR ERROR	ADDR OVFL ERROR	HEADER CRC ERROR	HEADER COMP ERROR	ECC HARD ERROR	WRITE CLOCK FAIL	FORMAT ERROR	PARITY ERROR	REG MOD RFSO	ILL REG	ILL FUNC
READ ONLY															

Bit	Name
-----	------

<b>15</b>	<b>DATA CHECK</b>
-----------	-------------------

When set, indicates that a data error has been detected during a READ operation, i.e. that the ECC generated does not match the ECC read from the sector.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01 > in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

<b>14</b>	<b>UNSAFE</b>
-----------	---------------

When set, indicates a condition exists that prevents proper operation such as low AC power or DEVICE CHECK <07> in the error 2 register is set.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01 > in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.



**13            OPERATION INCOMPLETE**

When set, indicates that the operation was not completed.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**12            DRIVE TIMING ERROR**

Set when a failure has been detected in the clocking or timing circuits of the drive.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**11            WRITE LOCK ERROR**

When set, indicates that the processor attempted to write on a write-protected drive (front panel switch set to write protect).

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**10            INVALID ADDRESS ERROR**

When set, indicates that the sector address specified by the desired cylinder and the desired sector/track address registers is invalid.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**09            ADDRESS OVERFLOW ERROR**

When set, indicates that the desired cylinder register has reached a count of more than  $822_{10}$ .

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control

## DISK REGISTERS

and status 2 register or INIT.

### **08            HEADER CRC ERROR**

When set, indicates that the header CRC generated does not match the CRC read from the sector.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **07            HEADER COMPARE ERROR**

When set, indicates that the sector reached by the drive did not match the address of the sector read from the header.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **06            ECC HARD ERROR**

When set, indicates that the data error cannot be corrected by the Error Correction Code (ECC) circuitry.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **05            WRITE CLOCK FAIL**

When set, indicates that the drive did not receive MASSBUS write clock signals from the controller during a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **04            FORMAT ERROR**

When set, indicates that the format (16-bit or 18-bit) of the disk pack or disk head assembly does not match the format of the drive.

The format of the drive is set by loading 16-BIT FORMAT <12> in the

offset register and the format of the pack or disk head assembly is written into the header field when the pack or disk head assembly is formatted.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**03            PARITY ERROR**

When set, indicates that a MASSBUS data parity error has been detected during a WRITE operation or a MASSBUS control bus parity error has been detected while writing a drive register.

A MASSBUS data parity error detected during a READ operation sets MASSBUS DATA PARITY ERROR <08> in the control and status 2 register. A MASSBUS control bus parity error detected while reading a drive register sets MASSBUS CONTROL BUS PARITY ERROR <13> in the control and status 1 register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**02            REGISTER MODIFICATION REFUSED**

When set, indicates that an attempt has been made to write any drive register except the attention summary register while the drive is performing an operation, i.e. the GO bit <00> in the control and status 1 register is set.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**01            ILLEGAL REGISTER**

When set, indicates an attempt has been made to read or write a non-existent drive register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a drive CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

## DISK REGISTERS

### 00 ILLEGAL FUNCTION

When set, indicates that an invalid function code has been loaded into FUNCTION CODE <05-01> in the control and status 1 register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a drive CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### ATTENTION SUMMARY REGISTER (AS)

776716 (PDP-11)

BYTE OFFSET = 10 (VAX)



Bit	Name
-----	------

15-08	NOT USED
-------	----------

07-00	ATTENTION BITS
-------	----------------

These bits correspond to ATTENTION <15> in the status register of disk drives 7-0.

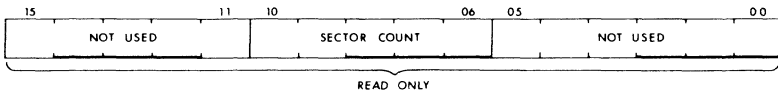
Individual bits are cleared by loading them with a 1 or by clearing ATTENTION <15> in the status register of the corresponding drive.

Also cleared by INIT.

### LOOK-AHEAD REGISTER (LA)

776720 (PDP-11)

BYTE OFFSET = 1C (VAX)



Bit	Name
-----	------

15-11	NOT USED
-------	----------

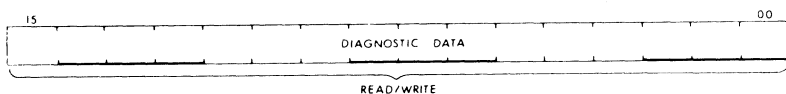
10-06	SECTOR COUNT
-------	--------------

These bits indicate the sector (0-31<sub>10</sub>) at which the heads are currently positioned.

# DISK REGISTERS

05-00 NOT USED

## DATA BUFFER REGISTER (RMDb) 776722 (PDP-11 ONLY)



**Bit Name**

### 15-00 DIAGNOSTIC DATA

This register is used for testing the controller. Up to eight words can be loaded into and read back from this register.

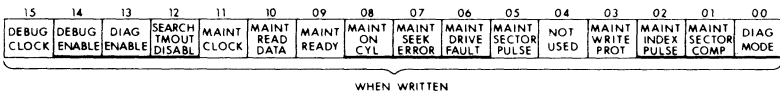
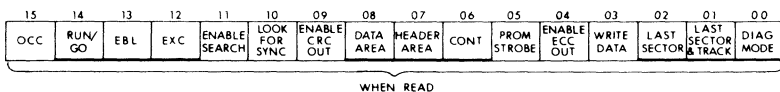
This register is not full and words may be loaded when INPUT READY <06> in the control and status 2 register is set.

This register has words to be read when OUTPUT READY <07> in the control and status 2 register is set.

## MAINTENANCE 1 REGISTER (MR1)

776724 (PDP-11)

BYTE OFFSET = C (VAX)

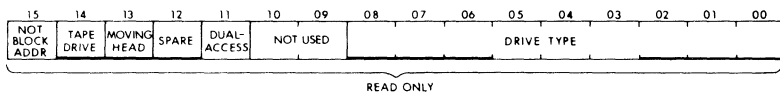


This register is used for diagnostic testing.

## DRIVE TYPE REGISTER (DT)

776726 (PDP-11)

BYTE OFFSET = 18 (VAX)



## DISK REGISTERS

**Bit            Name**

**15            NOT BLOCK ADDRESSED**

This bit is always 0.

**14            TAPE DRIVE**

This bit is always 0.

**13            MOVING HEAD**

This bit is always 1.

**12            SPARE**

This bit is always 0.

**11            DRIVE REQUEST REQUIRED (DUAL-ACCESS)**

When set, indicates that the selected drive is dual-ported.

When clear, indicates that the selected drive is single-ported.

**10-09        NOT USED**

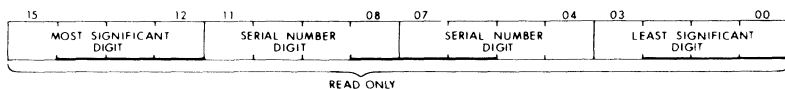
**08-00        DRIVE TYPE**

These bits indicate the drive type of the selected drive. Equal to  $026_8$  for an RM80,  $047_8$  for a single-ported RM05,  $027_8$  for a dual-ported RM05, and  $024_8$  for RM02/03.

### SERIAL NUMBER REGISTER (SN)

776730 (PDP-11)

BYTE OFFSET = 20 (VAX)

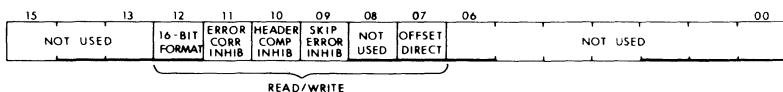


This register contains the four Least Significant Digits in binary coded decimal (BCD) of the selected drive.

### OFFSET REGISTER (OF)

776732 (PDP-11)

BYTE OFFSET = 24 (VAX)



## DISK REGISTERS

Bit	Name
-----	------

15-13	<b>NOT USED</b>
-------	-----------------

12	<b>16-BIT FORMAT</b>
----	----------------------

When set, causes the drive to use 16-bit word format.

11	<b>ERROR CORRECTION CODE INHIBIT</b>
----	--------------------------------------

When set, prevents the drive from performing error correction.

10	<b>HEADER COMPARE INHIBIT</b>
----	-------------------------------

When set, prevents the drive from verifying that it has reached the proper sector.

09	<b>SKIP SECTOR ERROR INHIBIT (RM80 only)</b>
----	--

When set, prevents the drive from setting SKIP SECTOR ERROR <05> in the error 2 register.

08	<b>NOT USED</b>
----	-----------------

07	<b>OFFSET DIRECTION</b>
----	-------------------------

This bit does not apply to the RM80.

When set, causes the drive to offset the heads 250 microinches toward the spindle.

When clear, causes the drive to offset the heads 250 microinches away from the spindle.

06-00	<b>NOT USED</b>
-------	-----------------

### DESIRED CYLINDER REGISTER (DC)

776734 (PDP-11)

BYTE OFFSET = 28 (VAX)



Bit	Name
-----	------

15-10	<b>NOT USED</b>
-------	-----------------

## DISK REGISTERS

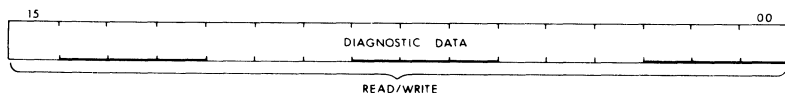
### 09-00 DESIRED CYLINDER ADDRESS

These bits select the cylinder address (0-560<sub>10</sub> for the RM80 or 0-822<sub>10</sub> for the RM05, RM02/03) at which the heads are to be positioned.

#### HOLDING REGISTER (HR)

776736 (PDP-11)

BYTE OFFSET = 2C (VAX)

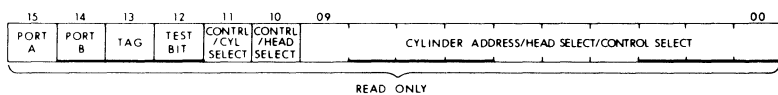


This register is used for diagnostic testing.

#### MAINTENANCE 2 REGISTER (MR2)

776740 (PDP-11)

BYTE OFFSET = 30 (VAX)

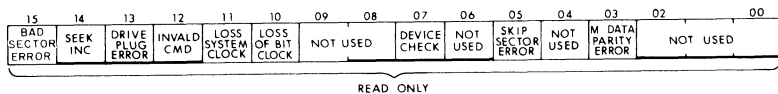


This register is used for diagnostic testing.

#### ERROR 2 REGISTER (ER2)

776742 (PDP-11)

BYTE OFFSET = 34 (VAX)



Bit	Name
-----	------

#### 15 BAD SECTOR ERROR

When set, the sector header field indicates that the sector is bad.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

#### 14 SEEK INCOMPLETE

When set, indicates that a SEEK operation has not yet been completed



## DISK REGISTERS

after 500 ms or that the heads have moved outside the recording field on the disk surface.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 13 DRIVE PLUG ERROR

When set, indicates that the drive number plug on the front panel has been removed.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared after replacing the plug by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 12 INVALID COMMAND

When set, indicates that DRIVE READY <07> or VOLUME VALID <06> in the drive status register are clear and that the processor issued a command other than READ-IN PRESET or PACK ACKNOWLEDGE.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 11 LOSS OF SYSTEM CLOCK

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 10 LOSS OF BIT CLOCK

When set, indicates that there have been no transitions in the bit clock for more than 400 ns.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 09-08 NOT USED

## DISK REGISTERS

### 07            **DEVICE CHECK**

When set, indicates a dc power supply failure or a head select fault.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 06            **NOT USED**

### 05            **SKIP SECTOR ERROR (RM80 only)**

When set, the sector header field indicates that the sector has been moved because it had a bad section.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 04            **NOT USED**

### 03            **MASSBUS DATA PARITY ERROR**

When set, indicates that a MASSBUS data parity error has been detected during a READ operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

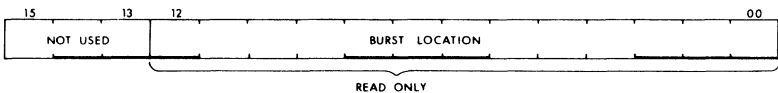
Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 02-00        **NOT USED**

## **ECC POSITION REGISTER (EC1)**

**776744 (PDP-11)**

**BYTE OFFSET = 38 (VAX)**



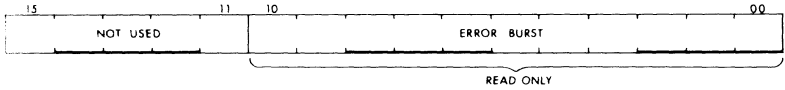
Bit	Name
-----	------

15-13	<b>NOT USED</b>
-------	-----------------

12-00	<b>BURST LOCATION</b>
-------	-----------------------

These bits specify the location in the record of the first bit of the error burst in the error pattern register.

**ECC PATTERN REGISTER (EC2)  
776746 (PDP-11)  
BYTE OFFSET=3C (VAX)**



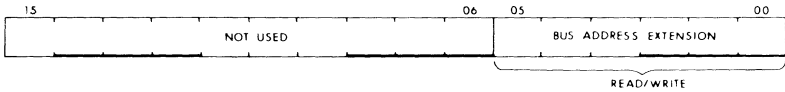
**Bit Name**

**15-11 NOT USED**

**10-00 ERROR BURST**

These bits are the 11-bit error correction burst that the software uses to correct the bad data in the record. The starting bit position is specified by the ECC position register.

**BUS ADDRESS EXTENSION REGISTER (BAE) 776750 (PDP-11/70 ONLY)**



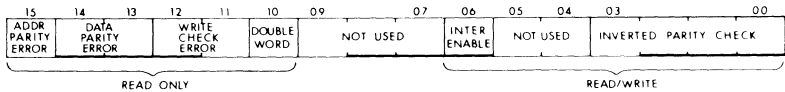
**Bit Name**

**15-06 NOT USED**

**05-00 BUS ADDRESS EXTENSION**

These bits contain the high-order six bits of the bus address. Refer to the bus address register for more detail.

**CONTROL AND STATUS 3 REGISTER (CS3) 776752 (PDP-11/70 ONLY)**



**Bit Name**

**15 ADDRESS PARITY ERROR**

When set, indicates that memory has detected a parity error on the

## DISK REGISTERS

address and control lines during a data transfer.

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 14-13      DATA PARITY ERROR

When set, indicates that a parity error has been detected on data from memory when the RH70 is performing a WRITE or WRITE CHECK command.

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 12-11      WRITE CHECK ERROR

Set when the controller is performing a WRITE CHECK operation and a word on the disk does not match the corresponding word in memory.

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 10          DOUBLE WORD

When set, indicates that the last memory transfer was a double word.

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 09-07      NOT USED

### 06          INTERRUPT ENABLE

Setting this bit sets INTERRUPT ENABLE <06> in the control and status 1 register.

### 05-04      NOT USED

### 03-00      INVERTED PARITY CHECK

These bits are used to control the parity circuits in the controller for diagnostic testing.

## RP06 REGISTERS

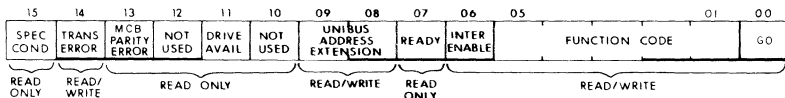
The RJP06 subsystems described in Chapter 2 have 20 registers, the RWP06 subsystems have 22 registers, and the REP06 and RGP06 subsystems have 16 registers plus the MASSBUS adapter registers. Following are the applicable register drawings and bit definitions. These register diagrams and bit definitions refer to both PDP-11 and VAX configurations unless noted. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the MASSBUS adapter registers.

Device registers on VAX MASSBUSes are located in a floating space starting at byte offset 400 from the base and extending to byte offset 7FC from the same base. Each of the up to eight devices supported by an MBA has a 128 byte space assigned to it. For example, the space for unit 0 would be from byte offset 400 to 47F and the space for unit 1 would be from byte offset 480 to 4FF. The byte offset bases are assigned according to the unit plug on the device. The range of byte offset bases for each of the up to eight devices supported by an MBA are as follows: 400, 480, 500, 580, 600, 680, 700, and 780. The VAX byte offsets shown here are relative to the base of the device registers.

## CONTROL AND STATUS 1 REGISTER (CS1)

776700 (PDP-11)

BYTE OFFSET=0 (VAX)



**Bit**                      **Name**

### 15                      SPECIAL CONDITION (PDP-11 ONLY)

Set by TRANSFER ERROR <14> or MASSBUS CONTROL BUS PARITY ERROR <13> in the control and status 1 register, or ATTENTION <15> in any of the drive status registers.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

Cleared by resetting the error bit that caused SPECIAL CONDITION to set.

### 14                      TRANSFER ERROR (PDP-11 only)

Set by any of the following bits in the control and status 2 register: DATA LATE <15>, WRITE CHECK ERROR <14>, PARITY ERROR

<13>, NON-EXISTENT DRIVE <12>, NON-EXISTENT MEMORY <11>, PROGRAM ERROR <10>, MISSED TRANSFER <09>, or MASSBUS DATA PARITY ERROR <08>.

Sets SPECIAL CONDITION <15>.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or by loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**13 MASSBUS CONTROL BUS PARITY ERROR (PDP-11 ONLY)**

Set when a parity error is detected while reading a drive register. A parity error detected while writing a drive register sets PARITY ERROR <03> in the error 1 register.

Sets SPECIAL CONDITION <15>.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or by loading a DATA TRANSFER command into FUNCTION CODE <05-01>

Also cleared by INIT.

**12 NOT USED**

**11 DRIVE AVAILABLE (PDP-11 ONLY)**

When set, indicates that the selected drive is present, turned on, and not being used by the other MASSBUS port.

**10 NOT USED**

**09-08 UNIBUS ADDRESS EXTENSION (PDP-11 ONLY)**

Loading these bits loads UNIBUS address bits <17, 16>. In the PDP-11/70 these bits can also be loaded by the bus address extension register.

Refer to the bus address register for more detail.

Cleared by loading with zeros.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**07 READY (PDP-11 ONLY)**

When set, indicates that the controller is ready to accept a command.

Generates an interrupt when the READY bit is set if INTERRUPT ENABLE <06> is also set.

Cleared while the controller is executing a command.

## DISK REGISTERS

### 06 INTERRUPT ENABLE (PDP-11 ONLY)

When set, generates an interrupt if READY <07> or SPECIAL CONDITION <15> is also set.

In the PDP-11/70 this bit is the same as INTERRUPT ENABLE <06> in the control and status 3 register.

Cleared when the interrupt is serviced by the processor.

Also cleared by INIT.

### 05-01 FUNCTION CODE

Loading these bits with one of the function codes listed below causes the selected drive to perform the corresponding operation. The GO bit <00> resets at the end of each operation.

61 <sub>8</sub>	WRITE DATA
51 <sub>8</sub>	WRITE CHECK DATA
63 <sub>8</sub>	WRITE HEADER AND DATA
53 <sub>8</sub>	WRITE CHECK HEADER AND DATA
71 <sub>8</sub>	READ DATA
73 <sub>8</sub>	READ HEADER AND DATA
05 <sub>8</sub>	SEEK
07 <sub>8</sub>	RECALIBRATE
17 <sub>8</sub>	RETURN TO CENTERLINE
15 <sub>8</sub>	OFFSET
31 <sub>8</sub>	SEARCH
03 <sub>8</sub>	UNLOAD
13 <sub>8</sub>	RELEASE MASSBUS PORT
21 <sub>8</sub>	READ-IN PRESET
23 <sub>8</sub>	PACK ACKNOWLEDGE
11 <sub>8</sub>	DRIVE CLEAR
01 <sub>8</sub>	NO OPERATION

### 00 GO

This bit resets at the end of each operation specified by FUNCTION CODE <05-01> .





## DISK REGISTERS

**Bit                      Name**

---

**15-13                      NOT USED**

**12-08                      TRACK ADDRESS**

These bits are loaded with a number (0-18<sub>10</sub>) which specifies the track on which the data transfer is to start.

The number is incremented by the drive at the end of sector 21.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or loading a DRIVE CLEAR command into FUNCTION CODE <05-01 > in the control and status 1 register.

Also cleared by INIT.

**07-05                      NOT USED**

**04-00                      SECTOR ADDRESS**

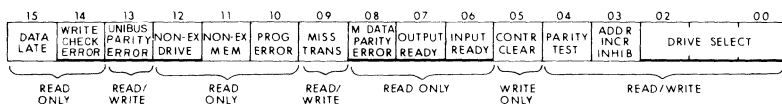
These bits are loaded with a number (0-21<sub>10</sub>) which specifies the sector in which the DATA TRANSFER is to start.

The number is incremented by the drive after each sector has been transferred.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or loading a DRIVE CLEAR command into FUNCTION CODE <05-00> in the control and status 1 register.

Also cleared by INIT.

### CONTROL AND STATUS 2 REGISTER (CS2) 776710 (PDP-11 ONLY)



**Bit                      Name**

---

**15                      DATA LATE**

Set when the controller is unable to supply a data word during a WRITE operation or accept a data word during a READ operation at the time that the drive requests a transfer.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**14 WRITE CHECK ERROR**

Set when the controller is performing a WRITE CHECK operation and a word on the disk does not match the corresponding word in memory.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**13 UNIBUS PARITY ERROR**

Set if a UNIBUS data parity error is detected during a WRITE operation. The bus address register will contain the address +2 (address +4 for PDP-11/70 systems) of the memory word with the parity error unless BUS ADDRESS INCREMENT INHIBIT <03> is not set.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**12 NON-EXISTENT DRIVE**

Set when a READ or WRITE operation attempt fails because the drive selected by DRIVE SELECT <02-00> does not exist or is turned off.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**11 NON-EXISTENT MEMORY**

Set when the controller attempts to transfer data into or from a memory address specified by the bus address register which does not exist. The bus address register will contain the address +2 (address +4 for PDP-11/70 systems) of the memory location that does not exist.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**10 PROGRAM ERROR**

Set when the program attempts to load a new command into FUNCTION CODE <05-01> in the control and status 1 register when READY <07> in the control and status 1 register is not set, i.e. when the controller is not ready to accept a command. The new command will not be loaded.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**09 MISSED TRANSFER**

Set if the drive does not respond to a DATA TRANSFER command, usually because ERROR SUMMARY <14> in the drive status register is set.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**08 MASSBUS DATA PARITY ERROR**

Set when a MASSBUS data parity error is detected during a READ operation. A parity error detected during a WRITE operation sets PARITY ERROR <03> in the error 1 register.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**07 OUTPUT READY**

This bit is used only for testing the controller.

When set, indicates that the data buffer register contains a word and may be read.

Cleared by reading the data buffer register or setting CONTROLLER CLEAR <05>.

Also cleared by INIT.

**06 INPUT READY**

This bit is used only for testing the controller.

## DISK REGISTERS

When set, indicates that the data buffer register is not full and may be loaded.

Cleared when the data buffer is fully loaded.

### 05 CONTROLLER CLEAR

When set, clears all error bits and initializes the controller and all of the drives.

### 04 PARITY TEST

When set, causes the controller to generate and check for even parity on the MASSBUS control bus and to generate even parity but check for odd parity on the MASSBUS data bus.

When clear, the controller generates and checks for odd parity on both the MASSBUS control bus and the MASSBUS data bus.

Cleared by loading with a 0.

Also cleared by setting CONTROLLER CLEAR <05> or INIT.

### 03 UNIBUS ADDRESS INCREMENT INHIBIT

When set, prevents the controller from incrementing the bus address register during a data transfer. Therefore, all data words are read from or written into the same memory location.

Cleared by loading with a 0.

Also cleared by setting CONTROLLER CLEAR <05> or INIT.

### 02-00 DRIVE SELECT

These bits are loaded to select the disk drive (0-7). This address is set by the numbered address plug in the drive.

## DRIVE STATUS REGISTER (DS)

776712 (PDP-11)

BYTE OFFSET = 4 (VAX)

15	14	13	12	11	10	09	08	07	06	05	04			03	02	01	00
ATTN	ERROR SUM	POS IN PROG	MED ON-LINE	WRITE LOCK	LAST SECTOR ACCESS TRANS	DUAL- ACCESS ENABLED	DRIVE PRES	DRIVE READY	VOLUME VALID	NOT USED			OFFSET MODE				
READ ONLY																	

**Bit**                      **Name**

### 15 ATTENTION (ATTN, ATA)

When set, indicates that an error or some unusual condition exists in the drive.

Sets SPECIAL CONDITION <15> in the control and status 1 register. Cleared by loading any command into FUNCTION CODE <05-01> in the control and status 1 register if ERROR SUMMARY <14> is not set. Cleared by loading the DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or by loading a 1 into the appropriate bit position in the attention summary register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**14 ERROR SUMMARY**

Set by any bit in the error 1, error 2, or error 3 registers. When set, the drive will accept no commands other than DRIVE CLEAR. Sets ATTENTION <15>. Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or setting CONTROLLER CLEAR <05> in the control and status 2 register. Also cleared by INIT.

**13 POSITIONING IN PROGRESS**

Set when the selected drive is performing a positioning operation (SEEK, OFFSET, RETURN TO CENTERLINE, RECALIBRATE, UNLOAD, and SEARCH). Cleared at the end of the operation.

**12 MEDIUM ON-LINE**

Set when the selected drive has a disk pack mounted, is on-line, and ready to execute a command. A change in the state of MEDIUM ON-LINE sets ATTENTION <15> and generates an interrupt.

**11 WRITE LOCK**

When set, indicates that the selected drive is write-protected (write protect switch on front panel is set).

**10 LAST SECTOR TRANSFERRED**

When set, indicates that cylinder 814, track 18, sector 21 (the last addressable sector) has been read or written.

**09 DUAL-ACCESS ENABLED (PROGRAMMABLE)**

When set, indicates that the port select switch on the selected drive is in the A/B position and that the drive is available to both MASSBUS ports.

## DISK REGISTERS

### 08 DRIVE PRESENT

When set, indicates that the selected drive is turned on.

### 07 DRIVE READY

Set when the selected drive is ready to execute a command.

### 06 VOLUME VALID

When clear, indicates that the drive has been put off-line and then on-line and that the disk pack may have been changed.

Cleared by the drive coming on-line.

Set by PACK ACKNOWLEDGE or READ-IN PRESET command.

### 05 DIFFERENCE EQUALS 1

Set when the drive has detected a value equal to 1 in the difference counter during a head load sequence.

Cleared by file ready at the completion of a head load sequence.

### 04 DIFFERENCE LESS THAN 64

Set when the drive has detected a value less than 64 in the difference counter during the reverse seek of the head load sequence.

Cleared by file ready at the completion of a head load sequence.

### 03 GO REVERSE

Set when the drive has detected a go reverse signal during a head load sequence.

Cleared by file ready at the completion of a head load sequence.

### 02 DRIVE TO INNER GUARD BAND

Set when the drive has detected the drive-to-inner-guard-band signal during a head load sequence.

Cleared by file ready at the completion of a head load sequence.

### 01 DRIVE FORWARD 20 IN/S

Set when the drive has detected a DF20 signal during a head load sequence.

Cleared by file ready at the completion of a head load sequence.

### 00 DRIVE FORWARD 5 IN/S

Set when the drive has detected a DF5 signal while in head load mode after a sequence start pulse was recognized.

Cleared by file ready at the completion of a head load sequence.

## DISK REGISTERS

### ERROR 1 REGISTER (ER1)

776714 (PDP-11)

BYTE OFFSET=8 (VAX)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	UNSAFE	OP INC	DRIVE TIMING ERROR	WRITE LOCK ERROR	INVLD ADDR ERROR	ADDR OVFL ERROR	HEADER CRC ERROR	HEADER COMP ERROR	ECC HARD ERROR	WRITE CLOCK FAIL	FORMAT ERROR	PARITY ERROR	REG MOD RFSD	ILL REG	ILL FUNC
READ ONLY															

**Bit            Name**

---

**15            DATA CHECK**

When set, indicates that a data error has been detected during a READ operation, i.e. that the ECC generated does not match the ECC read from the sector.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**14            UNSAFE**

Set when any of the unsafe bits in the error 1 or error 2 registers is set.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**13            OPERATION INCOMPLETE**

When set, indicates that the operation was not completed, i.e. that there was no data detected for three or more index pulses.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**12            DRIVE TIMING ERROR**

Set when a failure has been detected in the clocking or timing circuits of the drive.

Sets ERROR SUMMARY <14> in the drive status register.

## DISK REGISTERS

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 11            **WRITE LOCK ERROR**

When set, indicates that the processor attempted to write on a write-protected drive (front panel switch set to write protect).

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 10            **INVALID ADDRESS ERROR**

When set, indicates that the sector address specified by the desired cylinder and the desired sector/track address registers is invalid.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 09            **ADDRESS OVERFLOW ERROR**

When set, indicates that the desired cylinder register has reached a count of more than  $814_{10}$ .

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 08            **HEADER CRC ERROR**

When set, indicates that the header CRC generated does not match the CRC read from the sector.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.



## DISK REGISTERS

### 07           **HEADER COMPARE ERROR**

When set, indicates that the sector reached by the drive did not match the address of the sector read from the header.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 06           **ECC HARD ERROR**

When set, indicates that the data error cannot be corrected by the Error Correction Code (ECC) circuitry.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 05           **WRITE CLOCK FAIL**

When set, indicates that the drive did not receive MASSBUS write clock signals from the controller during a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 04           **FORMAT ERROR**

When set, indicates that the format (16-bit or 18-bit) of the disk pack does not match the format of the drive.

The format of the drive is set by loading FORMAT 22 <12> in the offset register and the format of the pack is written into the header field when the pack is formatted.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 03           **PARITY ERROR**

When set, indicates that a MASSBUS data parity error has been detected during a WRITE operation or a MASSBUS control bus parity

## *DISK REGISTERS*

error has been detected while writing a drive register.

A MASSBUS data parity error detected during a READ operation sets MASSBUS DATA PARITY ERROR <08> in the control and status 2 register. A MASSBUS control bus parity error detected while reading a drive register sets MASSBUS CONTROL BUS PARITY ERROR <13> in the control and status 1 register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **02 REGISTER MODIFICATION REFUSED**

When set, indicates that an attempt has been made to write any drive register except the attention summary register while the drive is performing an operation, i.e. the GO bit <00> in the control and status 1 register is set.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **01 ILLEGAL REGISTER**

When set, indicates an attempt has been made to read or write a non-existent drive register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a drive CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **00 ILLEGAL FUNCTION**

When set, indicates that an invalid function code has been loaded into FUNCTION CODE <05-01> in the control and status 1 register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a drive CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

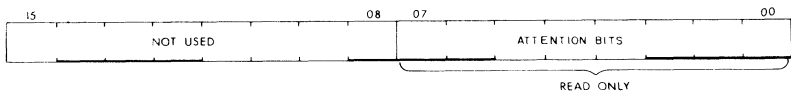
Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

## DISK REGISTERS

### ATTENTION SUMMARY REGISTER (AS)

776716 (PDP-11)

BYTE OFFSET = 10 (VAX)



Bit	Name
-----	------

15-08	NOT USED
-------	----------

07-00	ATTENTION BITS
-------	----------------

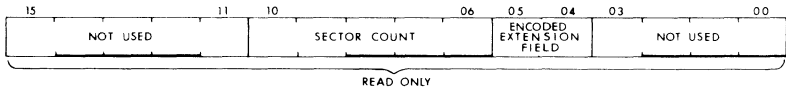
These bits correspond to ATTENTION <15> in the status register of disk drives 7-0.

Individual bits are cleared by loading them with a 1 or by clearing ATTENTION <15> in the status register of the corresponding drive. Also cleared by INIT.

### LOOK-AHEAD REGISTER (LA)

776720 (PDP-11)

BYTE OFFSET = 1C (VAX)



Bit	Name
-----	------

15-11	NOT USED
-------	----------

10-06	SECTOR COUNT
-------	--------------

These bits indicate that sector (0-21<sub>10</sub>) at which the heads are currently positioned.

05-04	ENCODED EXTENSION FIELD
-------	-------------------------

These bits indicate the section of the current sector at which the heads are currently positioned.

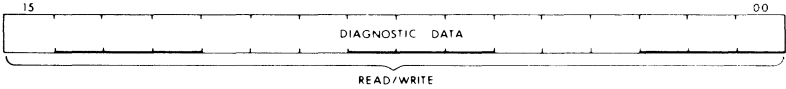
A value of 0<sub>2</sub> indicates that the heads are positioned at the first fifth of the sector, 1<sub>2</sub> indicates the second fifth, 2<sub>2</sub> the third fifth, and 3<sub>2</sub> indi-

## DISK REGISTERS

icates that the heads are positioned more that four fifths of the way through the sector.

**03-00      NOT USED**

### DATA BUFFER REGISTER (DB) 776722 (PDP-11 ONLY)

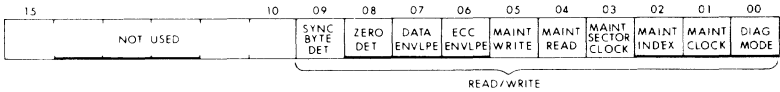


**Bit            Name**

**15-00      DIAGNOSTIC DATA**

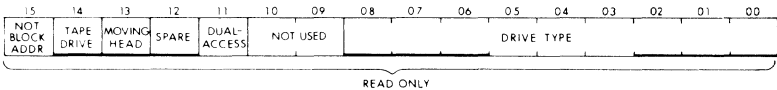
This register is used for testing the controller. Up to eight words can be loaded into and read back from this register.  
 This register is not full and words may be loaded when INPUT READY <06> in the control and status 2 register is set.  
 This register has words to be read when OUTPUT READY <07> in the control and status 2 register is set.

### MAINTENANCE REGISTER (MR) 776724 (PDP-11) BYTE OFFSET=C (VAX)



This register is used for diagnostic testing.

### DRIVE TYPE REGISTER (DT) 776726 (PDP-11) BYTE OFFSET=18



**Bit            Name**

**15            NOT BLOCK ADDRESSED**

This bit is always 0.

**14 TAPE DRIVE**

This bit is always 0.

**13 MOVING HEAD**

This bit is always 1.

**12 SPARE**

This bit is always 0.

**11 DRIVE REQUEST REQUIRED (DUAL-ACCESS)**

When set, indicates that the selected drive is dual-ported.

When clear, indicates that the selected drive is single-ported.

**10-09 NOT USED**

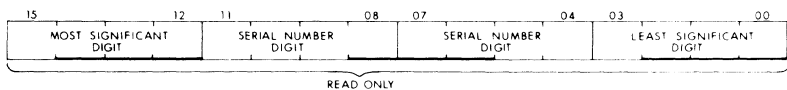
**08-00 DRIVE TYPE**

These bits indicate the drive type of the selected drive. Equal to 020022<sub>8</sub> for a single-ported RP06 and 024022<sub>8</sub> for a dual-ported RP06.

**SERIAL NUMBER REGISTER (SN)**

**776730 (PDP-11)**

**BYTE OFFSET=30**

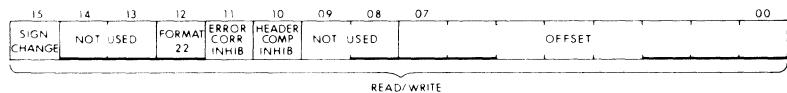


This register contains the four Least Significant Digits in binary coded decimal (BCD) of the selected drive.

**OFFSET REGISTER (OF)**

**776732 (PDP-11)**

**BYTE OFFSET=24 (VAX)**



## DISK REGISTERS

Bit	Name
-----	------

15	<b>SIGN CHANGE</b>
----	--------------------

This bit is used by the diagnostic that verifies head alignment with a CE pack mounted.

14-13	<b>NOT USED</b>
-------	-----------------

12	<b>FORMAT 22</b>
----	------------------

When set, causes the drive to use 16-bit word format (22 sectors per track).

11	<b>ERROR CORRECTION CODE INHIBIT</b>
----	--------------------------------------

When set, prevents the drive from performing error correction.

10	<b>HEADER COMPARE INHIBIT</b>
----	-------------------------------

When set, prevents the drive from verifying that it has reached the proper sector.

09-08	<b>NOT USED</b>
-------	-----------------

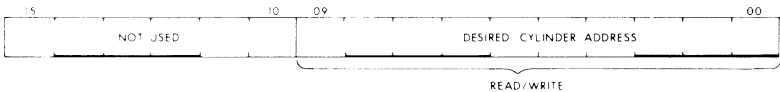
07-00	<b>OFFSET</b>
-------	---------------

These bits select how far off the center of the track the heads are to be set by the next OFFSET command.

### DESIRED CYLINDER REGISTER (DC)

776734 (PDP-11)

BYTE OFFSET = 28 (VAX)



Bit	Name
-----	------

15-10	<b>NOT USED</b>
-------	-----------------

09-00	<b>DESIRED CYLINDER ADDRESS</b>
-------	---------------------------------

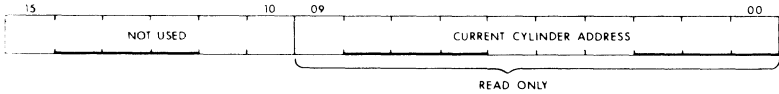
These bits select the cylinder address (0-814<sub>10</sub>) at which the heads are to be positioned.

## DISK REGISTERS

### CURRENT CYLINDER REGISTER (CC)

776736 (PDP-11)

BYTE OFFSET = 2C (VAX)



Bit	Name
-----	------

15-10	NOT USED
-------	----------

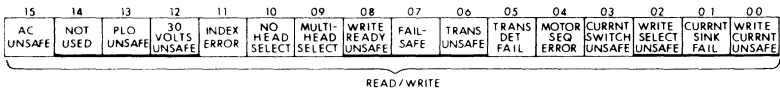
09-00	CURRENT CYLINDER ADDRESS
-------	--------------------------

When the heads are not moving, these bits indicate at which cylinder the heads are positioned.

### ERROR 2 REGISTER (ER2)

776740 (PDP-11)

BYTE OFFSET = 20 (VAX)



Bit	Name
-----	------

15	AC UNSAFE
----	-----------

When set, indicates that the drive has detected loss or interruption of AC power.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

14	NOT USED
----	----------

## DISK REGISTERS

### 13 PHASE-LOCKED OSCILLATOR UNSAFE

When set, indicates that the drive has detected loss of synchronization of the read/write phase-locked oscillator (PLO).

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 12 30 VOLTS UNSAFE

When set, indicates that the drive has detected loss of the 30 volt DC power supply.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 11 INDEX ERROR

When set, indicates that the drive has detected a missing or invalid index pulse.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 10 NO HEAD SELECTION

When set, indicates that a READ or WRITE command has been issued but that no head has been selected.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 09 MULTIPLE HEAD SELECT

When set, indicates that the drive has detected that more than one head has been selected at the same time.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.



## *DISK REGISTERS*

### **08 WRITE READY UNSAFE**

When set, indicates that the drive has received a WRITE command and the heads are not positioned at the cylinder.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **07 FAILSAFE ENABLED**

When set, indicates that the drive has detected that the circuit breaker in the 48 volt power supply has been turned off.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **06 TRANSITIONS UNSAFE**

When set, indicates that the drive has detected the absence of write transitions during a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **05 TRANSITIONS DETECTOR FAILURE**

When set, indicates that the drive has detected write transitions while performing an operation other than a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **04 MOTOR SEQUENCE ERROR**

When set, indicates that the drive has detected a Solid State Relay (SSR) failure, power sequence failure, or brush-in-pack error during a disk start-up sequence.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by manually restarting the drive.

**03            CURRENT SWITCH UNSAFE**

When set, indicates that the drive has detected an incorrect write current level during a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**02            WRITE SELECT UNSAFE**

When set, indicates that both even-side and odd-side heads are enabled for a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**01            CURRENT SINK FAILURE**

When set, indicates that the current sink is operating but the drive is not performing a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**00            WRITE CURRENT UNSAFE**

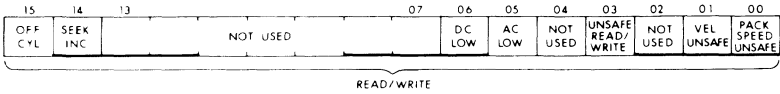
When set, indicates that the drive has detected write current while performing an operation other than a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**ERROR 3 REGISTER (ER3)**  
**776742 (PDP-11)**  
**BYTE OFFSET=34 (VAX)**



Bit	Name
-----	------

<b>15</b>	<b>OFF CYLINDER</b>
-----------	---------------------

When set, indicates that the drive has detected that the heads are not properly positioned at the cylinder.

Sets SEEK INCOMPLETE <14>.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

<b>14</b>	<b>SEEK INCOMPLETE</b>
-----------	------------------------

When set, indicates that a SEEK operation has not yet been completed after 100 ms.

Causes the drive to perform a RECALIBRATE operation and clear the current cylinder address register.

This bit cannot be reset until the drive completes its recovery procedure, approximately 1 s.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

<b>13-07</b>	<b>NOT USED</b>
--------------	-----------------

<b>06</b>	<b>DC LOW</b>
-----------	---------------

When set, indicates that loss of 5 volt DC power in the device control logic (DCL) of the drive has been detected.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

## DISK REGISTERS

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **05 AC LOW**

When set, indicates that a loss of AC input power to the device control logic (DCL) of the drive has been detected.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **04 NOT USED**

### **03 UNSAFE READ/WRITE**

When set, indicates that the heads have been retracted and prevents execution of READ, WRITE, or any positioning commands.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **02 NOT USED**

### **01 VELOCITY UNSAFE**

When set, indicates that the drive has detected excessive head positioner velocity.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **00 PACK SPEED UNSAFE**

When set, indicates that the disk pack speed is 80% less than normal and that the heads have not yet been retracted.

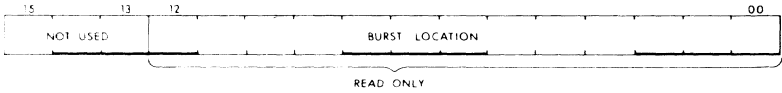
Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading with a 0 or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

## DISK REGISTERS

### ECC POSITION REGISTER (EC1) 776744 (PDP-11) BYTE OFFSET=38 (VAX)



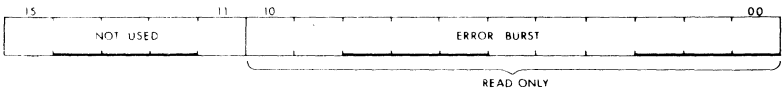
Bit	Name
-----	------

15-13	NOT USED
-------	----------

12-00	BURST LOCATION
-------	----------------

These bits specify the location in the record of the first bit of the error burst in the error pattern register.

### ECC PATTERN REGISTER (EC2) 776746 (PDP-11) BYTE OFFSET=3C (VAX9)



Bit	Name
-----	------

15-11	NOT USED
-------	----------

10-00	ERROR BURST
-------	-------------

These bits are the 11-bit error correction burst that the software uses to correct the bad data in the record. The starting bit position is specified by the ECC position register.

### BUS ADDRESS EXTENTION REGISTER (BAE) 776750 (PDP-11/70 ONLY)



## DISK REGISTERS

**Bit            Name**

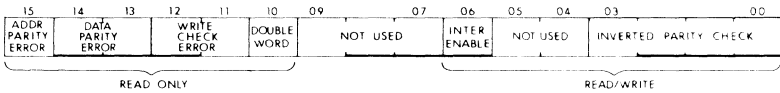
---

**15-06        NOT USED**

**05-00        BUS ADDRESS EXTENSION**

These bits contain the high-order six bits of the bus address. Refer to the bus address register for more detail.

### CONTROL AND STATUS 3 REGISTER (CS3) 776752 (PDP-11/70 ONLY)



**Bit            Name**

---

**15            ADDRESS PARITY ERROR**

When set, indicates that memory has detected a parity error on the address and control lines during a data transfer.

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**14-13        DATA PARITY ERROR**

When set, indicates that a parity error has been detected on data from memory when the RH70 is performing a WRITE or WRITE CHECK command.

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**12-11        WRITE CHECK ERROR**

Set when the controller is performing a WRITE CHECK operation and a word on the disk does not match the corresponding word in memory.

## DISK REGISTERS

Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 10            **DOUBLE WORD**

When set, indicates that the last memory transfer was a double word. Cleared by loading a DATA TRANSFER or DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 09-07        **NOT USED**

### 06            **INTERRUPT ENABLE**

Setting this bit sets INTERRUPT ENABLE <06> in the control and status 1 register.

### 05-04        **NOT USED**

### 03-00        **INVERTED PARITY CHECK**

These bits are used to control the parity circuits in the controller for diagnostic testing.

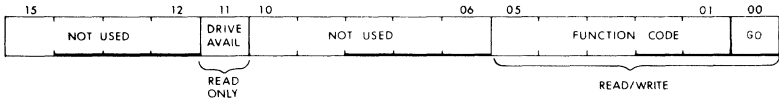
## **RP07 REGISTERS**

The REP07 disk subsystems described in Chapter 2 are supported by VAX-11/780 systems only. Following are the applicable register drawings and bit definitions. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the MASSBUS adapter registers.

Device registers on VAX MASSBUSes are located in a floating space starting at byte offset 400 from the base and extending to byte offset 7FC from the same base. Each of the up to eight devices supported by an MBA has a 128 byte space assigned to it. For example, the space for unit 0 would be from byte offset 400 to 47F and the space for unit 1 would be from byte offset 480 to 4FF. The byte offset bases are assigned according to the unit plug on the device. The range of byte offset bases for each of the up to eight devices supported by an MBA are as follows: 400, 480, 500, 580, 600, 680, 700, and 780. The VAX byte offsets shown here are relative to the base of the device registers.

## DISK REGISTERS

### CONTROL AND STATUS 1 REGISTER (RPCS1) BYTE OFFSET=0



**Bit            Name**

---

**15-12        NOT USED**

**11            DRIVE AVAILABLE**

When set, indicates that the selected drive is present, turned on, and not being used by the other MASSBUS port.

**10-06        NOT USED**

**05-01        FUNCTION CODE**

Loading these bits with one of the function codes listed below causes the selected drive to perform the corresponding operation.

6 <sub>1</sub>	WRITE DATA
5 <sub>1</sub>	WRITE CHECK DATA
6 <sub>3</sub>	FORMAT TRACK
5 <sub>3</sub>	WRITE CHECK HEADER AND DATA
6 <sub>5</sub>	WRITE TRACK DESCRIPTOR
7 <sub>1</sub>	READ DATA
7 <sub>3</sub>	READ HEADER AND DATA
7 <sub>5</sub>	READ TRACK DATA DESCRIPTOR
0 <sub>5</sub>	SEEK
0 <sub>7</sub>	RECALIBRATE
3 <sub>1</sub>	SEARCH



## DISK REGISTERS

- 13<sub>8</sub>            RELEASE MASSBUS PORT
- 21<sub>8</sub>            READ-IN PRESET
- 11<sub>8</sub>            DRIVE CLEAR
- 35<sub>8</sub>            MICRODIAGNOSTIC  
Initiates the microdiagnostic routine specified in the maintenance register.
- 23<sub>8</sub>            NO OPERATION
- 15<sub>8</sub>            OFFSET  
Only sets OFFSET MODE <00> in the drive status register. The RP07 cannot perform OFF-SET operations.
- 17<sub>8</sub>            RETURN TO CENTERLINE  
Generates an interrupt and clears OFFSET MODE <00> in the drive status register but does not actually return the heads to the centerline of the track because the RP07 cannot perform OFFSET operations.
- 01<sub>8</sub>            NO OPERATION
- 00            GO

This bit resets at the end of each operation specified by FUNCTION CODE <05-01>.

### DRIVE STATUS REGISTER (RPDS) BYTE OFFSET=4

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATTN	ERROR SUM	POS IN PROG	MED ON-LINE	WRITE LOCK	LAST BLOCK TRANS	DUAL-ACCESS ENABLED	DRIVE PRES	DRIVE READY	VOLUME VALID	NOT USED			INTER-LEAVED SECTORS	EARLY WARN	OFFSET MODE

READ ONLY

**Bit            Name**

**15            ATTENTION (ATA)**

When set, indicates that an error or some unusual condition exists in the drive.

## DISK REGISTERS

Cleared by loading any command into FUNCTION CODE <05-00> in the control and status 1 register if ERROR SUMMARY <14> is not set. Cleared by loading the DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or by loading a 1 into the appropriate bit position in the attention summary register.

### 14 ERROR SUMMARY

Set by any bit in the error 1, error 2, or error 3 registers.

When set, the drive will accept no commands other than DRIVE CLEAR.

Sets ATTENTION <15>.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 13 POSITIONING IN PROGRESS

Set when the selected drive is performing a positioning operation.

Cleared at the end of the operation.

### 12 MEDIUM ON-LINE

Set when the selected drive is on-line and ready to execute a command.

A change in the state of MEDIUM ON-LINE sets ATTENTION <15> and generates an interrupt.

### 11 WRITE LOCK

When set, indicates that the selected drive is write-protected (the write protect switch on the front panel is set).

### 10 LAST BLOCK TRANSFERRED

When set, indicates that cylinder 629, track 31, sector 49 (the last addressable sector) has been read or written.

### 09 DUAL-ACCESS ENABLED

When set, indicates that the port select switch on the selected drive is in the A/B position and that the drive is available to both MASSBUS ports.

### 08 DRIVE PRESENT

When set, indicates that the selected drive is turned on.

## DISK REGISTERS

### 07            **DRIVE READY**

Set when the selected drive is ready to execute a command.

### 06            **VOLUME VALID**

This bit is always a 1.

### 05-03        **NOT USED**

### 02            **INTERLEAVED SECTORS**

When set, indicates that the non-interleaved sectors jumper on J26 is not installed on the backpanel.

### 01            **EARLY WARNING**

When set, indicates that the drive has detected insufficient air flow or is almost overtemperature. If the drive gets any hotter, it will turn itself off.

### 00            **OFFSET MODE**

Set by executing an OFFSET command (the only function of the OFFSET command in the RP07).

## **ERROR 1 REGISTER (RPER1) BYTE OFFSET=8**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA CHECK	UNSAFE	OP INC	DRIVE TIMING ERROR	WRITE LOCK ERROR	INVLD ADDR ERROR	ADDR OVFL ERROR	HEADER CRC ERROR	HEADER COMP ERROR	ECC HARD ERROR	WRITE CLOCK FAIL	FORMAT ERROR	PARITY ERROR	REG MOD RFS	ILL REG	ILL FUNC

⏟  
READ ONLY

<b>Bit</b>	<b>Name</b>
------------	-------------

---

### 15            **DATA CHECK**

When set, indicates that a READ operation has detected a data error, i.e. that the ECC generated does not match the ECC read from the sector.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 14            **UNSAFE**

Set when any unsafe condition is detected including READ/WRITE

## *DISK REGISTERS*

UNSAFE 3 <13>, READ/WRITE UNSAFE 2 <12>, READ/WRITE UNSAFE 1 <11> in the error 2 register, or DC UNSAFE <05> in the error 3 register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **13            OPERATION INCOMPLETE**

When set, indicates that the drive did not find the correct sector within three revolutions or that it failed to detect an index pulse for three revolutions.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **12            DRIVE TIMING ERROR**

Set when a failure has been detected in the clocking or timing circuits of the drive.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **11            WRITE LOCK ERROR**

When set, indicates that the processor attempted to write on a write-protected drive (front panel switch set to write protect).

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **10            INVALID ADDRESS ERROR**

When set, indicates that the execution of a command was attempted when the sector address specified by the desired cylinder or the desired sector/track address registers is invalid.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**09 ADDRESS OVERFLOW ERROR**

When set, indicates that the desired cylinder register has reached a count of more than  $629_{10}$ .

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**08 HEADER CRC ERROR**

When set, indicates that the header CRC generated does not match the CRC read from the sector.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**07 HEADER COMPARE ERROR**

When set, indicates that the desired address did not match the address read from the header.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**06 ECC HARD ERROR**

When set, indicates that the data error cannot be corrected by the Error Correction Code (ECC) circuitry.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**05 WRITE CLOCK FAIL**

When set, indicates that the drive did not receive MASSBUS write clock signals from the controller during a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**04           FORMAT ERROR**

When set, indicates that the format (16-bit or 18-bit) of the disk head assembly does not match the format of the drive.

The format of the drive is set by loading 16-BIT FORMAT <12> in the offset register. The format of the disk head assembly is written into the header field when the disk head assembly is formatted.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**03           PARITY ERROR**

When set, indicates that a MASSBUS data parity error has been detected during a WRITE operation or a control bus parity error has been detected while writing a drive register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**02           REGISTER MODIFICATION REFUSED**

When set, indicates that an attempt has been made to write any drive register except the attention summary register while the drive is performing an operation, i.e. the GO bit <00> in the control and status 1 register is set.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**01           ILLEGAL REGISTER**

When set, indicates an attempt has been made to read or write an illegal drive register.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**00           ILLEGAL FUNCTION**

When set, indicates that an invalid function code has been loaded into FUNCTION CODE <05-01> in the control and status 1 register.

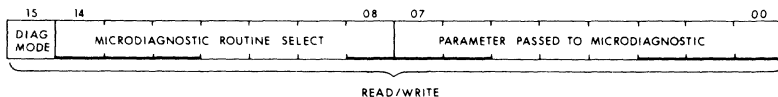
Sets ERROR SUMMARY <14> in the drive status register.

## DISK REGISTERS

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

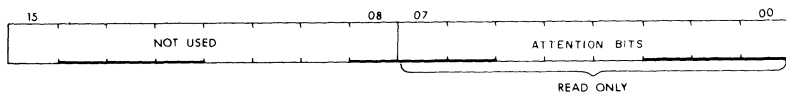
Also cleared by INIT.

### MAINTENANCE REGISTER (RPMR1) BYTE OFFSET = C



This register is used for diagnostic testing.

### ATTENTION SUMMARY REGISTER (RPAS) BYTE OFFSET = 10



Bit	Name
-----	------

15-08	NOT USED
-------	----------

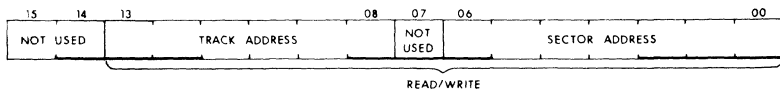
07-00	ATTENTION BITS
-------	----------------

These bits correspond to ATTENTION <15> in the status register of disk drives 7-0.

Individual bits are cleared by loading them with a 1 or by clearing ATTENTION <15> in the status register of the corresponding drive.

Also cleared by INIT.

### DESIRED SECTOR/TRACK ADDRESS REGISTER (RPDA) BYTE OFFSET = 14



## DISK REGISTERS

**Bit                      Name**

---

**15-14                      NOT USED**

**13-08                      TRACK ADDRESS**

These bits are loaded with a number (0-31<sub>10</sub>) which specifies the track on which the data transfer is to start.

The number is incremented by the drive at the end of sector 49.

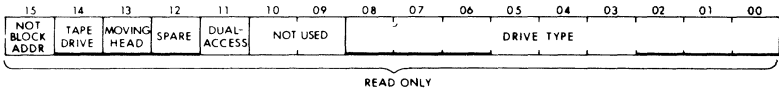
**07                              NOT USED**

**05-00                      SECTOR ADDRESS**

These bits are loaded with a number (0-49<sub>10</sub>) which specifies the sector in which the data transfer is to start.

The number is incremented by the drive after each sector has been transferred.

### DRIVE TYPE REGISTER (RPDT) BYTE OFFSET = 18



**Bit                              Name**

---

**15                              NOT BLOCK ADDRESSED**

This bit is always 0.

**14                              TAPE DRIVE**

This bit is always 0.

**13                              MOVING HEAD**

This bit is always 1.

**12                              SPARE**

This bit is always 0.

**11                              DUAL-ACCESS**

When set, indicates that the selected drive is dual-ported.

When clear, indicates that the selected drive is single-ported.

**10-09                      NOT USED**

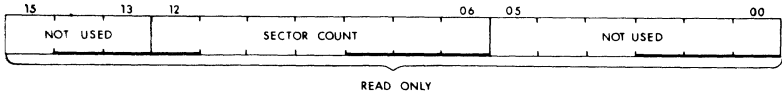


## DISK REGISTERS

### 08-00 DRIVE TYPE

These bits indicate the drive type of the selected drive. Equal to 042<sub>8</sub> for the RP07.

### LOOK-AHEAD REGISTER (RPLA) BYTE OFFSET=1C



**Bit**            **Name**

---

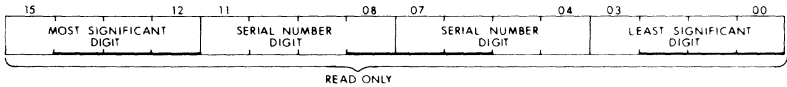
**15-13**        **NOT USED**

**12-06**        **SECTOR COUNT**

These bits indicate the sector (0-49<sub>10</sub>) at which the heads are currently positioned.

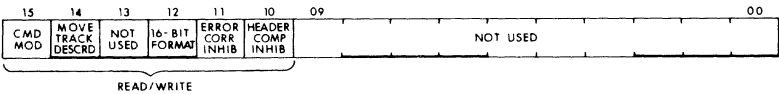
**05-00**        **NOT USED**

### SERIAL NUMBER REGISTER (RPSN) BYTE OFFSET=20



This register contains the four Least Significant Digits in binary coded decimal (BCD) of the selected drive.

### OFFSET REGISTER (RPOF) BYTE OFFSET=24



**Bit**            **Name**

---

**15**            **COMMAND MODIFIER**

When set, the READ TRACK DESCRIPTOR, WRITE TRACK DESCRIPTOR, and FORMAT TRACK commands can be executed. When clear, the execution of these commands is inhibited.

## DISK REGISTERS

### 14 MOVE TRACK DESCRIPTOR

When set, a WRITE TRACK DESCRIPTOR command causes the drive to write the track descriptor an additional 216 bytes (past the usual 128 bytes) after the index pulse.

### 13 NOT USED

### 12 16-BIT FORMAT

When set, causes the drive to use 16-bit word format.

### 11 ERROR CORRECTION INHIBIT

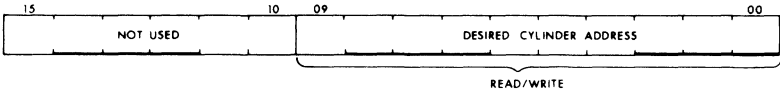
When set, prevents the drive from performing error correction.

### 10 HEADER COMPARE INHIBIT

When set, causes the drive to transfer the complete data field (512 bytes) when HEADER COMPARE ERROR <07> in the error 1 register is set.

### 09-00 NOT USED

## DESIRED CYLINDER REGISTER (RPDC) BYTE OFFSET = 28



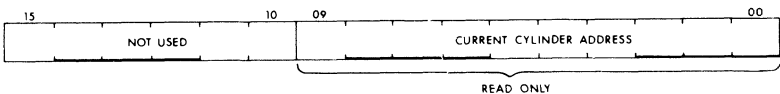
Bit	Name
-----	------

15-10	NOT USED
-------	----------

09-00	DESIRED CYLINDER ADDRESS
-------	--------------------------

These bits select the cylinder address (0-629<sub>10</sub>) at which the heads are to be positioned.

## CURRENT CYLINDER REGISTER (RPCC) BYTE OFFSET = 2C



## DISK REGISTERS

**Bit            Name**

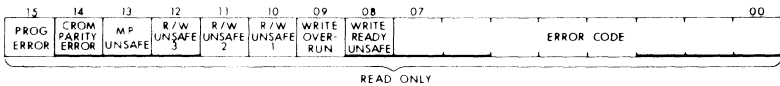
---

**15-10        NOT USED**

**09-00        CURRENT CYLINDER ADDRESS**

When the heads are not moving, these bits indicate at which cylinder the heads are positioned.

### **ERROR 2 REGISTER (RPER2) BYTE OFFSET = 30**



**Bit            Name**

---

**15            PROGRAM ERROR**

When set, indicates that the processor issued a WRITE TRACK DESCRIPTOR, READ TRACK DESCRIPTOR, or FORMAT TRACK command when COMMAND MODIFIER <15> in the offset register was not set.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**14            CROM PARITY ERROR**

When set, indicates that the microprocessor formatter has detected a Control ROM parity error.

Sets DEVICE CHECK <07> in the error 3 register and ERROR SUMMARY <14> in the drive status register.

Cleared by the microprocessor or by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

**13            MICROPROCESSOR UNSAFE**

When set, indicates that the 8080 microprocessor has stopped or is hung in a program loop.

Sets ERROR SUMMARY <14> in the drive status register.

## DISK REGISTERS

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 12 READ/WRITE UNSAFE 3

When set, indicates that the drive has detected write current when no write operation is in progress.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-00> in the control and status 1 register.

Also cleared by INIT.

### 11 READ/WRITE UNSAFE 2

When set, indicates that more than one head has been selected.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 10 READ/WRITE UNSAFE 1

When set, indicates that no write transitions have been detected during a WRITE operation.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 09 WRITE OVERRUN

When set, indicates that the drive has detected write current at both the leading and trailing edges of an index pulse.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### 08 WRITE READY UNSAFE

When set, indicates that the drive has detected write current when the heads are not centered on the track.

Sets ERROR SUMMARY <14> in the drive status register.

Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

## DISK REGISTERS

### 07-00      ERROR CODE

These bits contain the microdiagnostic error code from the 8080 microprocessor. This same code is displayed on the display panel.

### ERROR 3 REGISTER (RPER3) BYTE OFFSET = 34

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BAD SECTOR ERROR	SEEK INC	DEFECT SKIP ERROR	WRITE CURRNT FAIL	CONTRL LOGIC FAIL	LOSS OF BIT CLOCK	LOSS CYL ERROR	MP HAND- SHAKE	DEVICE CHECK	INDEX UNSAFE	DC UNSAFE	SEKDES DATA FAIL	DATA PARITY ERROR	SYNC BYTE ERROR	SYNC CLOCK FAIL	RUN TIME- OUT
<div style="text-align: center; border-top: 1px solid black; border-bottom: 1px solid black; padding: 2px 0;"> <span style="font-size: small;">READ ONLY</span> </div>															

**Bit            Name**

#### 15            BAD SECTOR ERROR

When set, the sector header field indicates that the sector is bad.  
 Sets ERROR SUMMARY <14> in the drive status register.  
 Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.  
 Also cleared by INIT.

#### 14            SEEK INCOMPLETE

When set, indicates that the drive has detected one of the following error conditions. The error conditions are specified by ERROR CODE <07-00> in the error 2 register.  
 When set, causes the drive to perform a RECALIBRATE operation and clear the current cylinder address register.  
 Sets ERROR SUMMARY <14> in the drive status register.  
 Cleared by loading a DRIVE CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.  
 Also cleared by INIT.

- 0A            SEEK operation too long.
- 0B            Guard band detected during SEEK operation.
- 0C            SEEK operation overshoot.
- 44            Guard band detection failure during RECALIBRATE operation.
- 45            Reference gap or guard band pattern detection failure during RECALIBRATE operation.

## DISK REGISTERS

46            Seek error during RECALIBRATE operation.

4A            Heads have attempted to land in guard band during RECALIBRATE operation.

### 13            **DEFECT SKIP ERROR**

When set, indicates that the a defect skip calculation has produced an invalid value.

### 12            **WRITE CURRENT FAILURE**

When set, indicates that the drive failed to detect write current after Write Gate was enabled.

### 11            **CONTROL LOGIC FAILURE**

When set, indicates that an attempt has been made to write the 8080 communications register when the register is full or a 2901 interrupt failure has been detected.

### 10            **LOSS OF BIT CLOCK**

When set, indicates that an END branch signal has not been detected within a specific time interval or that an END branch signal failed to negate after a new value was loaded into the 2901 byte count register.

### 09            **LOSS OF CYLINDER ERROR**

When set, indicates that movement of the head positioner has exceeded the cylinder boundary limits in Track Following mode.

### 08            **MICROPROCESSOR HANDSHAKE FAILURE**

When set, indicates that the 8080 microprocessor has failed to respond to a command.

### 07            **DEVICE CHECK**

When set, indicates that one or more of bits <15-08> in the error 2 register or bits <15-00> in the error 3 register are set.

### 06            **INDEX UNSAFE**

When set, indicates that an index error has been detected during a FORMAT TRACK or WRITE TRACK DESCRIPTOR operation.

### 05            **DC UNSAFE**

When set, indicates that the drive has detected low DC voltage.

## DISK REGISTERS

### 04 SERDES DATA FAILURE

When set, indicates that a timing failure relating to the drive data buffer has been detected.

### 03 DATA PARITY ERROR

When set, indicates that a data parity error has been detected during a WRITE operation.

### 02 SYNC BYTE ERROR

When set, indicates that the sync byte associated with a data field or defect skip has not been found.

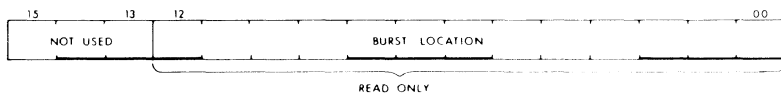
### 01 SYNC CLOCK FAILURE

When set, indicates that the sync clock counter has not reached zero within the time allowed for the function.

### 00 RUN TIMEOUT

When set, indicates that the drive has not detected a RUN signal on the MASSBUS within 30 ms from when GO <00> was set in the control and status 1 register.

## ECC POSITION REGISTER (RPEC1) BYTE OFFSET=38



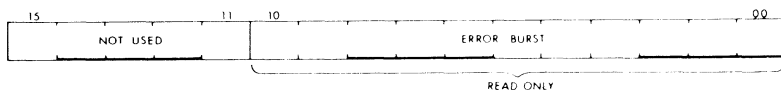
Bit	Name
-----	------

15-13	NOT USED
-------	----------

12-00	BURST LOCATION
-------	----------------

These bits specify the location in the record of the first bit of the error burst in the error pattern register.

## ECC PATTERN REGISTER (RPEC2) BYTE OFFSET=3C



## MAGNETIC TAPE REGISTERS

Bit	Name
-----	------

---

15-11	NOT USED
-------	----------

10-00	ERROR BURST
-------	-------------

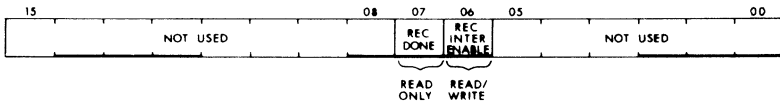
These bits are the 11-bit error correction burst that the software uses to correct the bad data in the record. The starting bit position is specified by the ECC position register.

## MAGNETIC TAPE REGISTERS

### TU58 REGISTERS

The TU58 cartridge tape subsystem described in Chapter 3 uses a DL11-E or a DL11-W to interface to the UNIBUS. Following are the applicable register drawings and bit definitions of the DL11-E and DL11-W registers when used with the TU58.

### RECEIVER STATUS REGISTER (RCSR) 776500



Bit	Name
-----	------

---

15-08	NOT USED
-------	----------

07	RECEIVER DONE
----	---------------

When set, indicates that a byte of data from the TU58 is in the receiver data buffer register and is ready to be read.

Generates an interrupt if RECEIVER INTERRUPT <06> is also set.

Cleared by reading the receiver data buffer register.

Also cleared by INIT.

06	RECEIVER INTERRUPT ENABLE
----	---------------------------

When set, allows an interrupt to occur when the RECEIVER DONE <07> bit is also set.

Cleared by loading with a 0.

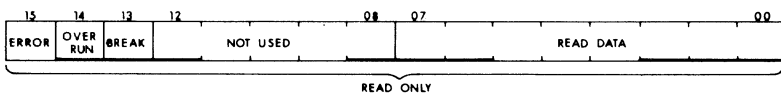
Also cleared by INIT.

05-00	NOT USED
-------	----------



## MAGNETIC TAPE REGISTERS

### RECEIVER DATA BUFFER REGISTER (RBUF) 776502



**Bit            Name**

---

**15            ERROR**

Set if either the OVERRUN <14> or BREAK <13> bit is set.  
Cleared by resetting either the OVERRUN <14> or BREAK <13> bit.

**14            OVERRUN**

Set when a byte of read data is loaded into READ DATA <07-00> (overwriting the previous byte) before the last byte has been read by the processor.

**13            BREAK**

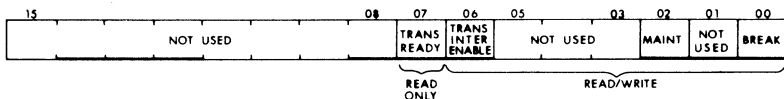
When set, indicates that the TU58 is sending a continuous BREAK signal.

**12-08        NOT USED**

**07-00        READ DATA**

These bits contain one byte (8 bits) of data to be read from the tape. Data can be read only when RECEIVER DONE <07> in the receiver status register is set.

### TRANSMITTER STATUS REGISTER (XCTSR) 776504



**Bit            Name**

---

**15-08        NOT USED**

**07            TRANSMITTER READY**

When set, indicates that the transmitted data buffer register is ready to accept a byte of WRITE DATA <07-00> from the processor.

## MAGNETIC TAPE REGISTERS

Generates an interrupt if TRANSMITTER INTERRUPT ENABLE <06> is also set.

Also set by INIT.

### 06 TRANSMITTER INTERRUPT ENABLE

When set, allows an interrupt to occur when the TRANSMITTER READY <07> bit is also set.

Cleared by loading with a zero.

Also cleared by INIT.

### 05-03 NOT USED

### 02 MAINTENANCE

When set, causes data loaded into WRITE DATA <07-00> of the transmitted data buffer register to appear in READ DATA <07-00> of the receiver data buffer register.

Cleared by loading with a zero.

Also cleared by INIT.

### 01 NOT USED

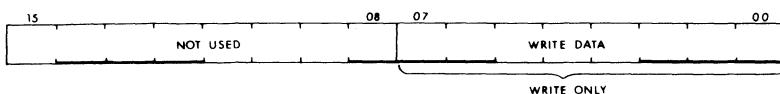
### 00 BREAK

When set, causes a BREAK signal to be sent to the TU58. When the TU58 receives the signal it immediately stops the current operation.

Cleared by loading with a zero.

Also cleared by INIT.

## TRANSMITTED DATA BUFFER REGISTER (XBUF) 776506



Bit	Name
-----	------

15-08	NOT USED
-------	----------

07-00	WRITE DATA
-------	------------

These bits contain one byte (8 bits) of data to be written on the tape. Data can be loaded only when TRANSMITTER READY <07> in the transmitter status register is set.

**TS11 REGISTERS AND EXTENDED STATUS WORDS**

The TS11 magnetic tape subsystems described in Chapter 3 have two registers: the Status Register and the Bus Address/Data Buffer Register. The TS11 also references five extended status words, which function like registers, and are stored in memory locations. Following are the applicable register and extended status word diagrams and bit definitions. These register diagrams and bit definitions refer to both PDP-11 and VAX configurations unless noted. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the UNIBUS adapter registers.

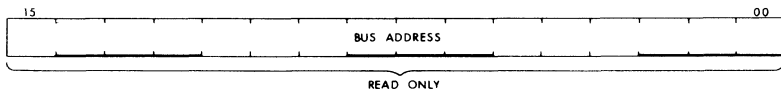
**BUS ADDRESS REGISTER (TSBA)**

772520 (Transport 0)

772524 (Transport 1)

772530 (Transport 2)

772534 (Transport 3)



**Bit            Name**

**15-00            BUS ADDRESS**

These bits contain the address of the last word the TS11 read from or wrote into memory. Bits <17-16> of the bus address may be read from BUS ADDRESS <09-08> in the status register.

**DATA BUFFER REGISTER (TSDB)**

772520 (Transport 0)

772524 (Transport 1)

772530 (Transport 2)

772534 (Transport 3)



**Bit            Name**

**15-02            COMMAND ADDRESS**

Loading these bits with the starting address of the control program

## MAGNETIC TAPE REGISTERS

causes the TS11 to read the program from memory and to execute it.

### 01-00      **COMMAND ADDRESS**

These bits correspond to bits <17-16> of the Command Address. Note that bits <01-02> of the Command Address are always 0.

### **STATUS REGISTER (TSSR)**

**772522 (Transport 0)**

**772526 (Transport 1)**

**772532 (Transport 2)**

**772536 (Transport 3)**

15	14	13	12	11	10	09	08	07	06	05	04	03	01	00
SPEC COND	UNIBUS PARITY ERROR	SERIAL BUS PARITY	REG MOD REF	NON- EXIST MEM	NEED BUFFER ADDR	BUS ADDR <17, 16>		READY	OFF- LINE	FATAL ERROR CLASS	TERMINATION CLASS		NOT USED	
READ ONLY														

**Bit            Name**

### 15            **SPECIAL CONDITION**

Set by UNIBUS PARITY ERROR <14>, SERIAL BUS PARITY ERROR <13>, REGISTER MODIFICATION REFUSED <12>, NON-EXISTENT MEMORY <11>, NEED BUFFER ADDRESS <10>, or TERMINATION CLASS <03-01> if it is equal to  $1_8-7_8$ .

Generates an interrupt if INTERRUPT ENABLE <07> in the last Command Word is also set.

Cleared by writing this register or by executing a TRANSPORT INITIALIZE command.

Also cleared by INIT.

### 14            **UNIBUS PARITY ERROR**

When set, indicates that the controller has detected a parity error in a word read from memory.

Sets SPECIAL CONDITION <15>.

Sets TERMINATION CLASS <03-01> to  $4_8$  or  $5_8$ .

Cleared by writing this register or by executing a TRANSPORT INITIALIZE command.

Also cleared by INIT.

### 13            **SERIAL BUS PARITY ERROR**

When set, indicates that the controller has detected a parity error in

## MAGNETIC TAPE REGISTERS

data received from the transport.

Sets SPECIAL CONDITION <15>.

Sets TERMINATION CLASS <03-01> to 7<sub>8</sub>.

Sets FATAL ERROR CLASS <05-04> to 2<sub>8</sub>.

Cleared by writing this register or by executing a TRANSPORT INITIALIZE command.

Also cleared by INIT.

### 12 REGISTER MODIFICATION REFUSED

When set, indicates that the bus address register is loaded but that READY <07> is not set.

Sets SPECIAL CONDITION <15>.

Cleared by writing this register or by executing a TRANSPORT INITIALIZE command.

Also cleared by INIT.

### 11 NON-EXISTENT MEMORY

When set, indicates that the TS11 has attempted to read a word from a non-existent address in memory.

Sets SPECIAL CONDITION <15>.

Cleared by writing this register or by executing a TRANSPORT INITIALIZE command.

Also cleared by INIT.

### 10 NEED BUFFER ADDRESS

When set, indicates that the TS11 needs a message buffer address to write status information into memory.

Sets SPECIAL CONDITION <15>.

Cleared by executing a SET CHARACTERISTICS command.

Also cleared by INIT.

### 09-08 BUS ADDRESS

These bits contain bits <17-16> of the bus address.

### 07 READY

When set, indicates that the TS11 is not busy and is ready to execute a command.

Generates an interrupt if INTERRUPT ENABLE <07> in the last Command Word is also set.

### 06 OFF-LINE

When set, indicates that the transport is off-line.

## MAGNETIC TAPE REGISTERS

### 05-04 FATAL ERROR CLASS

When SPECIAL CONDITION <15> is set and TERMINATION CLASS <03-01> is equal to 7<sub>8</sub>, these bits are valid. Error class codes are as follows:

- |                 |   |
|-----------------|---|
| 00 <sub>2</sub> | Indicates that the microdiagnostics have detected a failure. MICRODIAGNOSTIC ERROR CODE <15-08> in the Extended Status 3 Word specifies the failure.<br>Cleared by executing a TRANSPORT INITIALIZE command.<br>Also cleared by INIT. |
| 01 <sub>2</sub> | Indicates that an I/O sequencer CROM parity error has been detected.<br>Cleared by executing a TRANSPORT INITIALIZE command.<br>Also cleared by INIT.   |
| 10 <sub>2</sub> | Indicates that a microprocessor CROM parity error, an I/O silo parity error, or a serial bus parity error has been detected.<br>Cleared by INIT.  |
| 11 <sub>2</sub> | Indicates that a loss of AC power has been detected.<br>Cleared by INIT.  |

### 03-01 TERMINATION CLASS

When SPECIAL CONDITION <15> is set these bits are valid. Termination class codes are as follows:

- |                |           |  |
|----------------|-----------|--|
| 0 <sub>8</sub> | Normal    | When set, indicates that the operation has been successfully completed.  |
| 1 <sub>8</sub> | Attention | Set by a change in OFF-LINE <06> or a microdiagnostic failure. MICRODIAGNOSTIC ERROR CODE <15-08> in the Extended Status 3 Word specifies the failure. |



## MAGNETIC TAPE REGISTERS

Bit	Name
-----	------

15	<b>ACKNOWLEDGE</b>
----	--------------------

When set, enables the TS11 to write status words in memory locations into the status address specified by the last SET CHARACTERISTICS command.

14	<b>CLEAR STATUS CHANGE</b>
----	----------------------------

When set, clears STATUS CHANGE <04> (VCK on front panel) in the Extended Status 0 Word.

13	<b>OPPOSITE</b>
----	-----------------

When set, causes the TS11 to reverse the execution sequence of the reread commands.

12	<b>SWAP BYTES</b>
----	-------------------

When set, causes the TS11 to reverse the order in which bytes are packed into or unpacked from 16-bit words during READ and WRITE operations.

11-08	<b>COMMAND CODE</b>
-------	---------------------

Refer to the description of COMMAND CODE <04-00>.

07	<b>INTERRUPT ENABLE</b>
----	-------------------------

When set, generates an interrupt when either SPECIAL CONDITION <15> or READY <07> in the status register is set.

06-05	
-------	--

These bits are always 0.

04-00	<b>COMMAND CODE</b>
-------	---------------------

Loading bits <11-08> and <04-00> specifies the operation that the TS11 is to perform. The operation codes (with INTERRUPT ENABLE <07> set) are as follows:

0201 <sub>8</sub>	READ
-------------------	------

0601 <sub>8</sub>	READ BACKWARD
-------------------	---------------



## MAGNETIC TAPE REGISTERS

1201 <sub>8</sub>	REREAD (SPACE BACKWARD, READ FORWARD)
1601 <sub>8</sub>	READ BACKWARD NEXT (SPACE FORWARD, READ BACKWARD)
0205 <sub>8</sub>	WRITE
1205 <sub>8</sub>	WRITE RETRY (SPACE BACKWARD, ERASE GAP, WRITE)
2210 <sub>8</sub>	REWIND
0612 <sub>8</sub>	REWIND/UNLOAD

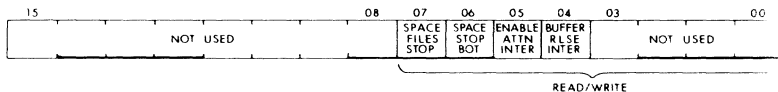
The following four commands use a two-word control program instead of the usual four-word control program. The first word is the Command Word and the second word contains a count of the number of blocks or files to be skipped.

0210 <sub>8</sub>	SPACE BLOCKS FORWARD
0610 <sub>8</sub>	SPACE BLOCKS BACKWARD
1210 <sub>8</sub>	SPACE FILES FORWARD Skips a specified number of tape marks.
1610 <sub>8</sub>	SPACE FILES BACKWARD Skips a specified number of tape marks.
0211 <sub>8</sub>	WRITE TAPE MARK
1211 <sub>8</sub>	WRITE TAPE MARK RETRY (SPACE BACKWARD, ERASE GAP, WRITE TAPE MARK)
0611 <sub>8</sub>	ERASE GAP Erases 3.2 inches of tape.
0213 <sub>8</sub>	TRANSPORT INITIALIZE
0204 <sub>8</sub>	SET CHARACTERISTICS Causes the TS11 to read the Characteristics Word and the status address from memory.

## MAGNETIC TAPE REGISTERS

- 0217<sub>8</sub>      **GET STATUS**  
 Causes the TS11 to write the five extended status words into memory starting at the status address specified by the last SET CHARACTERISTICS command. A GET STATUS command needs only a one-word control program.
- 1212<sub>8</sub>      **CLEAN**
- 0206<sub>8</sub>      **WRITE MICROPROCESSOR MEMORY**  
 Used only for diagnostic testing.
- 0212<sub>8</sub>      **STATUS BUFFER RELEASE**  
 Enables the TS11 to write the five extended status words into memory whenever there is a change in OFF-LINE <06> in the status register or a microdiagnostic failure is detected.

### CHARACTERISTICS WORD ADDRESS SPECIFIED BY THE LAST SET CHARACTERISTICS COMMAND



**Bit            Name**

**15-08        NOT USED**

**07            ENABLE SPACE FILES STOP**

When set while the TS11 is executing a SPACE FILES command causes the TS11 to stop when it detects two tape marks in a row (logical end of tape).

**06            ENABLE SPACE FILES STOP AT BOT**

When set, causes the TS11 to stop and set LOGICAL END OF TAPE

## MAGNETIC TAPE REGISTERS

<13> in the Extended Status 0 Word if 1) the transport is at BOT, and 2) a SPACE FILES FORWARD command is executed, and 3) the first record is a tape mark.

### 05            **ENABLE ATTENTION INTERRUPT**

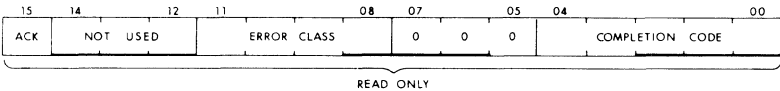
When set, the TS11 generates an interrupt if the transport goes on-line or off-line, i.e. STATUS CHANGE <04> in Extended Status 0 Word is set, or a microdiagnostic failure has been detected and the last command sent was a STATUS BUFFER RELEASE command.

### 04            **ENABLE STATUS BUFFER RELEASE INTERRUPT**

When set, the TS11 will not generate an interrupt after a STATUS BUFFER RELEASE command is executed.

### 03-00        **NOT USED**

## **STATUS HEADER WORD ADDRESS SPECIFIED BY LAST SET CHARACTERISTICS COMMAND**



**Bit            Name**

### 15            **ACKNOWLEDGE**

When set, indicates that the TS11 is no longer using the control program words so that the processor may rewrite them if desired.

### 14-12        **NOT USED**

### 11-08        **ERROR CLASS**

These bits contain codes which specify the type of error detected by the TS11. Error class codes are as follows:

00<sub>8</sub>            If COMPLETION CODE<04-00> is equal to 23<sub>8</sub>, the interrupt was caused by the transport going off-line or coming on-line.

## MAGNETIC TAPE REGISTERS

If COMPLETION CODE<04-00> is equal to  $21_8$ , a parity error has been detected, i.e. SERIAL BUS PARITY ERROR<13> in the status register is set.

- $04_8$  If COMPLETION CODE<04-00> is equal to  $23_8$ , a microdiagnostic failure has been detected.  
If COMPLETION CODE<04-00> is equal to  $21_8$ , the TS11 was unable to execute the command, i.e. ILLEGAL COMMAND <09> or ILLEGAL ADDRESS <08> in Extended Status 0 Word or NEED STATUS ADDRESS<10> in the status register is set.
- $10_8$  If COMPLETION CODE<04-00> is equal to  $21_8$ , the TS11 was unable to execute the command, i.e. WRITE LOCK ERROR <11> or NON-EXECUTABLE COMMAND <10> in Extended Status 0 Word is set.
- $14_8$  If COMPLETION CODE<04-00> is equal to  $21_8$ , a microdiagnostic failure has been detected.

### 07-05

These bits are always 0.

### 04-00 COMPLETION CODE

These bits contain codes which indicate whether or not the operation has been completed with or without error. The completion codes are as follows:

- $20_8$  Indicates that the operation has been completed without errors. However, TERMINATION CLASS<03-01> in the status register may be equal to  $2_8$ , indicating an unusual condition, not necessarily an error.
- $21_8$  Indicates that the operation has failed to execute.



**14            SHORT RECORD**

When set, indicates that 1) during a READ operation the record was shorter than the specified byte count, 2) a SPACE BLOCKS operation stopped after detecting a tape mark or BOT before skipping the specified number of blocks, 3) a SPACE FILES operation stopped after detecting BOT or two tape marks in a row if ENABLE SPACE FILES STOP<07> in the Characteristics Word is set.

**13            LOGICAL END OF TAPE**

When set, indicates that a SPACE FILES operation stopped after detecting two tape marks in a row or that a SPACE FILES FORWARD operation 1) started from BOT, and 2) the first record was a tape mark, and 3) ENABLE SPACE FILES STOP AT BOT <06> in the Characteristics Word is set.

**12            LONG RECORD**

When set, indicates that the record read was longer than the specified byte count.

**11            WRITE LOCK ERROR**

When set, indicates that the processor attempted a WRITE operation on a write-locked transport. Refer to the description of WRITE LOCK <02>.

**10            NON-EXECUTABLE COMMAND**

When set, indicates that the command could not be executed because 1) a backwards operation was attempted at BOT, 2) a tape motion operation was attempted when STATUS CHANGE<04> was set, 3) a tape motion operation was attempted when the transport was not on-line, ie. ON-LINE <06> is set or, 4) a WRITE operation was attempted on a write-locked transport.

**09            ILLEGAL COMMAND**

When set, indicates that the TS11 attempted to execute an invalid command.

**08            ILLEGAL ADDRESS**

When set, indicates that the address specified by the control program contains more than 18 bits or is odd (an even address is required).

## MAGNETIC TAPE REGISTERS

### 07 MOTION

When set, indicates that the capstan is moving.

### 06 ON-LINE

When set, indicates that the transport is on-line.

### 05 INTERRUPT ENABLE

When set, indicates that INTERRUPT ENABLE <07> in the last Command Word is set.

### 04 VOLUME CHECK

When set, indicates that the transport has gone off-line or come on-line (VOL VALID or VCK on front panel).

Generates an interrupt if ENABLE ATTENTION INTERRUPT <05> in the Characteristics Word is set.

Cleared by setting CLEAR STATUS CHANGE <14> in the Command Word.

### 03 PE ONLY TRANSPORT

This bit is always 1.

### 02 WRITE LOCK

When set, indicates that the tape reel does not have a file-protect ring.

### 01 BOT

When set, indicates that the tape is at BOT (Beginning Of Tape).

### 00 EOT

When set, indicates that the tape transport has passed the EOT (End Of Tape) marker.

## EXTENDED STATUS 1 WORD (XSTAT1) STATUS ADDRESS + 8

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DATA LATE	NOT USED	CORR DATA	CREASE DETECT	TRASH IN GAP	DESKEW BUFFER FAIL	SPEED CHECK	NOT USED	INVALID PRE- AMBLE	SYNC FAIL	INVALID POST- AMBLE	INVALID EOD	SHORT POST- AMBLE	LONG POST- AMBLE	INCOR DATA	MULT DEAD TRACK

READ ONLY

**Bit**                      **Name**

**15**                      **DATA LATE**

When set, indicates that the I/O silo has become full during a READ

## MAGNETIC TAPE REGISTERS

operation or empty during a WRITE operation.

**14 NOT USED**

**13 CORRECTABLE DATA**

When set, indicates that a data error was detected during a READ operation but was corrected on-the-fly.

**12 CREASE DETECTED**

When set, indicates that eight of the nine tracks went dead for a short distance (less than 0.1 in) while reading a record.

**11 TRASH IN THE GAP**

When set, indicates that extraneous data was detected in the inter-record gap.

**10 DESKEW BUFFER FAIL**

When set, indicates that one of the deskew buffers failed to set output ready within 20  $\mu$ s after being enabled. DEAD TRACK <08-00> in Extended Status 2 Word specifies which buffer failed.

**09 SPEED CHECK**

When set, indicates that the tape speed varied more than  $\pm 5\%$  during a WRITE operation.

**08 NOT USED**

**07 INVALID PREAMBLE**

When set, indicates that the preamble was shorter than 36 characters or longer than 44 characters or incorrectly encoded.

**06 SYNCHRONIZATION FAILURE**

When set, indicates that the formatter was unable to synchronize with the data rate in the preamble during a READ operation.

**05 INVALID POSTAMBLE**

When set, indicates that the postamble was not read or written correctly.



## MAGNETIC TAPE REGISTERS

### 04           INVALID END OF DATA

When set, indicates that eight or the nine tracks went dead while reading a record.

### 03           SHORT POSTAMBLE

When set, indicates that the postamble on a record is less than 38 characters long.

### 02           LONG POSTAMBLE

When set, indicates that the postamble on a record is more than 42 characters long.

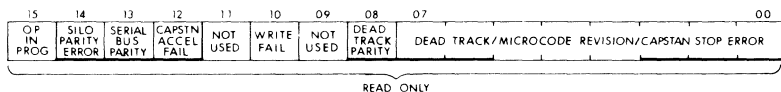
### 01           INCORRECTABLE DATA

When set, indicates that a data parity error was detected during a READ operation but there was no dead track to allow on-the-fly error correction or that a data parity error was detected during a WRITE operation.

### 00           MULTIPLE DEAD TRACK ERROR

When set, indicates that more than one dead track was detected during a READ operation.

## EXTENDED STATUS 2 WORD (XSTST2) STATUS ADDRESS +10



Bit	Name
-----	------

### 15           OPERATION IN PROGRESS

When set, indicates the tape is in motion.

### 14           SILO PARITY ERROR

When set, indicates that the microprocessor formatter has detected an error in its internal data silo.

### 13           SERIAL BUS PARITY ERROR

When set, indicates that the formatter detected a parity error in data received from the controller.



## MAGNETIC TAPE REGISTERS

### 07            **LIMIT EXCEEDED**

When set, indicates that the tension arm or arms moved too far during a tape motion operation. The tape must be reloaded manually.

### 06            **OPERATION INCOMPLETE**

When set, indicates that 25 feet of tape has been read or skipped (spaced) without detecting any data.

### 05            **REVERSE**

When set, indicates that the last command executed included a BACKWARD TAPE operation.

### 04            **CAPSTAN RESPONSE FAIL**

When set, indicates that the formatter detected no tachometer pulses within 5 ms after signaling the capstan to move.

### 03            **DENSITY CHECK**

When set, indicates that an invalid identification burst (IDB), indicating that the tape was not written in PE, was sensed at BOT (DENS ERROR or DCK on front panel). However, the tape can still be read if IDB is incorrect and the tape is actually written in PE.

### 02            **NOISE RECORD**

When set, indicates that data too short to be a record has been detected during a SPACE operation.

### 01            **LIMIT EXCEEDED STATICALLY**

When set, indicates that the tension arm or arms moved too far when the TS11 was idle. The tape must be reloaded manually.

### 00            **REVERSE INTO BOT**

When set, indicates that a backward operation past BOT has been attempted.

## **TU77/TE16 REGISTERS**

The TJU77 and TJE16 subsystems described in Chapter 3 have 20 registers, the TWU77 and TWE16 subsystems have 22, and the TEU77, TGU77, and TEE16 subsystems have 16 plus the MASSBUS adapter

## MAGNETIC TAPE REGISTERS

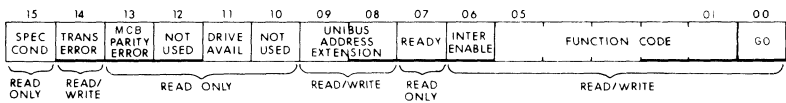
registers. Following are the applicable register drawings and bit definitions. These register diagrams and bit definitions refer to both PDP-11 and VAX configurations unless noted. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the MASSBUS adapter registers.

Device registers on VAX MASSBUSes are located in a floating space starting at byte offset 400 from the base and extending to byte offset 7FC from the same base. Each of the up to eight devices supported by an MBA has a 128 byte space assigned to it. For example, the space for unit 0 would be from byte offset 400 to 47F and the space for unit 1 would be from byte offset 480 to 4FF. The byte offset bases are assigned according to the unit plug on the device. The range of byte offset bases for each of the up to eight devices supported by an MBA are as follows: 400, 480, 500, 580, 600, 680, 700, and 780. The VAX byte offsets shown here are relative to the base of the device registers.

### CONTROL AND STATUS 1 REGISTER (MTCS1)

**772440 (PDP-11)**

**Byte Offset=0 (VAX)**



Bit	Name
-----	------

15	<b>SPECIAL CONDITION (PDP-11 only)</b>
----	--

Set by TRANSFER ERROR <14>, MASSBUS CONTROL BUS PARITY ERROR <13>, or ATTENTION <15> in the formatter status register. Generates an interrupt if INTERRUPT ENABLE <06> is also set. Cleared by resetting the error bit that caused SPECIAL CONDITION to set.

14	<b>TRANSFER ERROR (PDP-11 only)</b>
----	-------------------------------------

Set by any of the following bits in the control status 2 register: DATA LATE <15>, UNIBUS PARITY ERROR <13>, NON-EXISTENT FORMATTER <12>, NON-EXISTENT MEMORY <11>, PROGRAM ERROR <10>, MISSED TRANSFER <09>, or MASSBUS DATA PARITY ERROR <08>.

Sets SPECIAL CONDITION <15>.

## MAGNETIC TAPE REGISTERS

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or by loading a DATA TRANSFER command into FUNCTION CODE <05-01>

Also cleared by INIT.

### 13            **MASSBUS CONTROL BUS PARITY ERROR (PDP-11 only)**

Set when a parity error is detected while reading a formatter register. A parity error detected while writing a formatter register sets MASSBUS CONTROL BUS PARITY ERROR <03> in the error register. Sets SPECIAL CONDITION <15>.

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or by loading a DATA TRANSFER command into FUNCTION CODE <05-01>.

Also cleared by INIT.

### 12            **NOT USED**

### 11            **DRIVE AVAILABLE (PDP-11 only)**

When set, indicates that the selected formatter is present and turned on.

### 10            **NOT USED**

### 09-08        **UNIBUS ADDRESS EXTENSION (PDP-11 only)**

Loading these bits loads UNIBUS address bits <17, 16>. In the PDP-11/70 these bits can also be loaded by the bus address extension register.

Refer to the bus address register for more detail.

Cleared by loading with zeros.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 07            **READY (PDP-11 only)**

When set, indicates that the controller is ready to accept a command. Generates an interrupt when the READY bit is set if INTERRUPT ENABLE <06> is also set.

Cleared while the controller is executing a command.

### 06            **INTERRUPT ENABLE (PDP-11 only)**

When set, generates an interrupt if READY <07> or SPECIAL CONDITION <15> is also set.

In the PDP-11/70 this bit is the same as INTERRUPT ENABLE <06> in the control and status 3 register.



## MAGNETIC TAPE REGISTERS

**Bit            Name**

---

**15-01            BUS ADDRESS**

This register is loaded with the starting address where data is to be written from or read into memory .

For PDP-11 systems, except the PDP-11/70, the bus address is 18 bits. The low-order 16 bits are loaded by the bus address register and the high-order 2 bits are loaded by bits <09-08> in the control and status 1 register. During READ and WRITE FORWARD operations the bus address is incremented by two for each word transferred to or from memory. During a READ BACKWARD operation the bus address is decremented by two for each word transferred to memory.

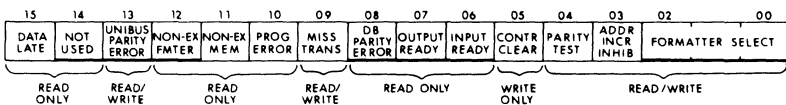
For PDP-11/70 systems only, the bus address is 22 bits. The low-order 16 bits are loaded by the bus address register and the high-order 6 bits are loaded by bits <05-01> in the bus address extension register. The PDP-11/70 uses double word transfers, i.e. two words at a time. During READ and WRITE FORWARD operations the bus address is incremented by four for each double word transferred to or from memory. During a READ BACKWARD operation the bus address is decremented by four for each double word transferred to memory. Cleared by loading with zeros.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**0                BUS ADDRESS**

This bit is always 0.

**CONTROL AND STATUS 2 REGISTER (MTCS2) 772450  
(PDP-11 ONLY)**



**Bit            Name**

---

**15                DATA LATE**

Set when the controller is unable to supply a data word during a WRITE operation or accept a data word during a READ operation at the time that the formatter requests a transfer.

## MAGNETIC TAPE REGISTERS

Sets TRANSFER ERROR <14> in the control and status 1 register.  
Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by INIT.

### **14 NOT USED**

### **13 UNIBUS PARITY ERROR**

Set if a UNIBUS data parity error is detected during a WRITE operation. The bus address register will contain the address +2 (address +4 for PDP-11/70 systems) of the memory word with the parity error unless BUS ADDRESS INCREMENT INHIBIT <03> is not set.  
Sets TRANSFER ERROR <14> in the control and status 1 register.  
Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by INIT.

### **12 NON-EXISTENT FORMATTER**

Set when a READ or WRITE operation attempt fails because the formatter selected by FORMATTER SELECT <02-00> does not exist or is turned off.  
Sets TRANSFER ERROR <14> in the control and status 1 register.  
Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by INIT.

### **11 NON-EXISTENT MEMORY**

Set when the controller attempts to transfer data into or from a memory address specified by the bus address register which does not exist. The bus address register will contain the address +2 (address +4 for PDP-11/70 systems) of the memory location that does not exist.  
Sets TRANSFER ERROR <14> in the control and status 1 register.  
Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.  
Also cleared by INIT.

### **10 PROGRAM ERROR**

Set when the program attempts to load a new command into FUNC-



## MAGNETIC TAPE REGISTERS

TION CODE <05-01> in the control and status 1 register when READY <07> in the control and status 1 register is not set, i.e. when the controller is not ready to accept a command. The new command will not be loaded.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **09 MISSED TRANSFER**

Set if the formatter does not respond to a DATA TRANSFER command, usually because ERROR SUMMARY <14> in the formatter status register is set.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **08 MASSBUS DATA PARITY ERROR**

Set when a MASSBUS data parity error is detected during a READ operation. A parity error detected during a WRITE operation sets MASSBUS DATA PARITY ERROR <05> in the error register.

Sets TRANSFER ERROR <14> in the control and status 1 register.

Cleared by setting CONTROLLER CLEAR <05> or loading a DATA TRANSFER command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by INIT.

### **07 OUTPUT READY**

This bit is used only for testing the controller.

When set, indicates that the data buffer register contains a word and may be read.

Cleared by reading the data buffer register or setting CONTROLLER CLEAR <05>.

Also cleared by INIT.

### **06 INPUT READY**

This bit is used only for testing the controller.

When set, indicates that the data buffer register is not full and may be loaded.

## MAGNETIC TAPE REGISTERS

Cleared when the data buffer is fully loaded.

### 05 CONTROLLER CLEAR

When set, clears all error bits and initializes the controller and the formatter.

### 04 PARITY TEST

When set, causes the controller to generate and check for even parity on the MASSBUS control bus and to generate even parity but check for odd parity on the MASSBUS data bus.

When clear, the controller generates and checks for odd parity on both the MASSBUS control bus and the MASSBUS data bus.

Cleared by loading with a 0.

Also cleared by setting CONTROLLER CLEAR <05> or INIT.

### 03 MEMORY ADDRESS INCREMENT INHIBIT

When set, prevents the controller from incrementing the bus address register during a data transfer. Therefore, all data words are read from or written into the same memory location.

Cleared by loading with a 0.

Also cleared by setting CONTROLLER CLEAR <05> or INIT.

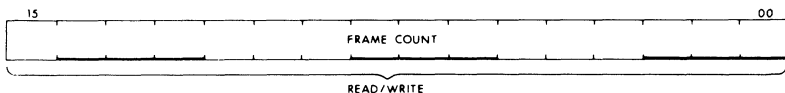
### 02-00 FORMATTER SELECT

These bits are loaded to select the formatter (only one formatter per controller). The usual formatter address is 0<sub>6</sub>. This address is set by the numbered address plug in the formatter.

## FRAME COUNT REGISTER (MTFC)

772446 (PDP-11)

Byte offset = 14 (VAX)



Before a WRITE operation can begin, this register must be loaded with the two's complement of the number of data bytes to be written. During the WRITE operation the frame count is incremented each time a byte is written onto the tape. The operation ends when the frame count reaches zero.

At the start of a READ operation, the formatter clears this register. During a READ operation, the frame count is incremented each time a

byte is read from the tape. At the end of the READ operation the frame count register contains a count of the number of bytes read.

Before a SPACE operation can begin, this register must be loaded with the two's complement of the number of records to be skipped. During the SPACE operation, the frame count is incremented each time a record is skipped. The operation ends when the frame count reaches zero.

**FORMATTER STATUS REGISTER (MTFS)**

**777 452 (PDP-11)**

**Byte offset = 4 (VAX)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
ATTN	ERROR SUM	POS IN PROG	MED ON-LINE	WRITE LOCK	EOT	NOT USED	FMTER PRES	FMTER READY	SLAVE STATUS CHANGE	PE STATUS	SLOW DOWN	ID BURST	TAPE MARK	BOT	SLAVE ATTN

READ ONLY

**Bit Name**

**15 ATTENTION (ATTN, ATA)**

When set indicates an error or some unusual condition in the formatter or tape transport.

Set by ERROR SUMMARY <14>, SLAVE STATUS CHANGE <06>, or EOT <10>.

Also set at the completion of the following operations: REWIND, REWIND/UNLOAD, ERASE GAP, WRITE TAPE MARK, SPACE FORWARD, and SPACE BACKWARD.

Sets SPECIAL CONDITION <15> in the control and status 1 register. Cleared by loading any command into FUNCTION CODE <05-00> in the control and status 1 register if ERROR SUMMARY <14> is not set. Cleared by loading the FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or by loading a 1 into the appropriate bit position in the attention summary register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

**14 ERROR SUMMARY**

Set by any bit in the error register.

When set, the formatter will accept no commands other than FORMATTER CLEAR.

Sets ATTENTION <15>.

Cleared by loading the FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register or setting

## MAGNETIC TAPE REGISTERS

CONTROLLER CLEAR <05> in the control and status 2 register.  
Also cleared by INIT.

### 13            **POSITIONING IN PROGRESS**

Set when the selected transport is performing a SPACE or REWIND operation.

Cleared at the end of an operation.

### 12            **MEDIUM ON-LINE**

Set when the selected transport has a tape loaded and is on-line and ready to execute a command.

A change in the status of MEDIUM ON-LINE sets SLAVE STATUS CHANGE <06>.

### 11            **WRITE LOCK**

Set when the tape loaded on the selected transport does not have a file-protect ring.

### 10            **END OF TAPE (EOT)**

Set when the selected transport has detected the EOT marker during forward tape motion.

Cleared when the transport has detected the EOT marker during backward tape motion.

The program should check to see if the EOT bit is set to avoid writing off the end of the tape.

### 09            **NOT USED**

### 08            **FORMATTER PRESENT**

When set, indicates that the selected formatter is connected to the processor.

### 07            **FORMATTER READY**

Set when the formatter is ready to accept a command.

If the selected transport is ready to accept a command, MEDIUM ON-LINE <12> is also set.

### 06            **SLAVE STATUS CHANGE**

When set indicates that one of the transports has gone on-line or off-line or has completed a REWIND operation.

Set by a change in the status of MEDIUM ON-LINE <12>.

Sets ATTENTION <15>.

## MAGNETIC TAPE REGISTERS

Cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register.

### 05 PE STATUS

When set, indicates that the selected transport is in PE mode (1600 b/in).

During a WRITE operation, set by DENSITY SELECT <10-08> in the tape control register.

When set during a READ operation, indicates that the formatter's auto density select circuit has detected a PE identification burst at BOT.

Clear when the selected transport is in NRZI mode (800 b/in).

### 04 SLOWING DOWN

When set, indicates that FORMATTER READY <07> is set but that the selected transport has not yet stopped the tape motion.

Cleared when the transport stops and MEDIUM ON-LINE <12> is set.

### 03 IDENTIFICATION BURST

When set, indicates that a PE identification burst was detected during the last operation.

### 02 TAPE MARK

When set, indicates that a tape mark was detected during the last operation.

Cleared by loading a TAPE MOTION or FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 01 BEGINNING OF TAPE (BOT)

When set, indicates that the tape on the selected transport is at BOT.

### 00 SLAVE ATTENTION

When set, indicates that the selected transport is on-line.

Sets MEDIUM ON-LINE <12>.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

# MAGNETIC TAPE REGISTERS

## ERROR REGISTER (MTER)

**772454 (PDP-11)**

**Byte Offset = 8 (VAX)**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CORR DATA/ CRC	UNSAFE	OP INC	CONTR TIMING ERROR	NON-EX FUNC	CORR SKEW/ ILL TM	FRAME COUNT	NON- STAND GAP	PE FORMAT/ LRC	INCORR DATA/ PARITY	M DATA PARITY ERROR	FORMAT SELECT	MCB PARITY ERROR	REG MOD RPSD	ILL REG	ILL FUNC
READ ONLY															

**Bit            Name**

### 15            CORRECTABLE DATA/CRC ERROR

In PE mode, this bit is set when an error is detected during a READ operation and the error was corrected on-the-fly and correct data sent to memory.

In NRZI mode, this bit is set when the CRC character read from the tape during a READ operation does not match the CRC character generated from the data read off the tape.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 14            UNSAFE

When set, indicates that a READ or WRITE operation has been attempted on a transport that is off-line, i.e. MEDIUM ON-LINE <12> in the formatter status register is not set.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 13            OPERATION INCOMPLETE

When set, indicates that the end of the record was not detected within seven seconds after the start of an operation.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

## MAGNETIC TAPE REGISTERS

### 12 CONTROLLER TIMING ERROR

When set, indicates that the formatter has not received a byte of data from the controller in time to write it in the proper location on the tape. Sets ERROR SUMMARY <14> in the formatter status register. Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 11 NON-EXECUTABLE FUNCTION

When set, indicates 1) that a WRITE operation has been attempted on a write-locked transport, i.e. WRITE-LOCK <11> in the formatter status register is set, 2) that a READ BACKWARD or SPACE BACKWARD operation has been attempted on a transport at BOT, i.e. BOT <01> in the formatter status register is set, 3) that a WRITE or SPACE operation has been attempted when the frame count register contains 0, or 4) that an attempt to write a NRZI record shorter than thirteen bytes has been made, i.e. that DENSITY SELECT <10-08> in the tape control register is equal to  $011_2$  and the frame count register contains less than  $13_{10}$ .

Sets ERROR SUMMARY <14> in the formatter status register. Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 10 CORRECTABLE SKEW/ILLEGAL TAPE MARK

In PE mode, this bit is set when excessive but correctable skew has been detected in the data read from the tape but correct data has been sent to memory.

In NRZI mode, this bit is set when the data read from the tape is similar to a NRZI tape mark, even when it is not actually a tape mark.

Sets ERROR SUMMARY <14> in the formatter status register. Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register. Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 09 FRAME COUNT ERROR

When set, indicates that a SPACE operation has ended and that the frame count register is not at zero, i.e. the transport has not skipped the correct number of blocks.

## MAGNETIC TAPE REGISTERS

Refer to the description of FRAME COUNT STATUS <14> in the tape control register for more detail.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **08 NON-STANDARD GAP**

When set, indicates that the read-after-write circuitry detected extraneous data written in the interrecord gap during a WRITE operation.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **07 PE FORMAT ERROR/LRC ERROR**

In PE mode, this bit is set when an invalid preamble or postamble has been detected.

In NRZI mode, this bit is set when the LRC character read from the tape does not match the LRC character generated from the data read off the tape.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **06 INCORRECTABLE DATA/VERTICAL PARITY ERROR**

When set, indicates that a data error has been detected during a DATA TRANSFER operation and that incorrect data has been transferred to memory or onto the tape.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### **05 MASSBUS DATA PARITY ERROR**

When set, indicates that a MASSBUS data parity error has been detected during a WRITE operation.



## MAGNETIC TAPE REGISTERS

A MASSBUS parity error detected during a READ operation sets MASSBUS DATA PARITY ERROR <08> in the control and status 2 register.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 04            **FORMAT SELECT ERROR**

When set, indicates that a DATA TRANSFER operation has been attempted with a invalid code in FORMAT SELECT <07-04> in the tape control register.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <00-05> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 03            **MASSBUS CONTROL BUS PARITY ERROR**

When set, indicates that a parity error has been detected while writing a formatter register.

A parity error detected while reading a formatter register sets MASSBUS CONTROL BUS PARITY ERROR <13> in the control and status register.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

### 02            **REGISTER MODIFICATION REFUSED**

When set, indicates that an attempt has been made to write any formatter register except the maintenance register or the attention summary register while the formatter is performing an operation, i.e. the GO bit <00> in the control and status 1 register is set.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

# MAGNETIC TAPE REGISTERS

## 01 ILLEGAL REGISTER

When set, indicates an attempt has been made to read or write a non-existent formatter register.

Sets ERROR SUMMARY <14> in the formatter status register.

Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

## 00 ILLEGAL FUNCTION

When set, indicates that an invalid function code has been loaded into FUNCTION CODE <05-01> in the control and status 1 register.

Sets ERROR SUMMARY <14> in the formatter status register.

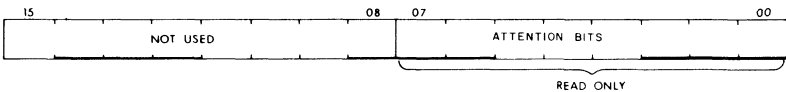
Cleared by loading a FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

## ATTENTION SUMMARY REGISTER (MTAS)

772456 (PDP-11)

Byte Offset=10 (VAX)



Bit	Name
-----	------

15-08	NOT USED
-------	----------

07-00	ATTENTION BITS
-------	----------------

On VAX systems that mix tape transports and disk drives on the same MBA, these bits correspond to ATTENTION <15> in the status registers for disk drives 7-0 or the tape formatter.

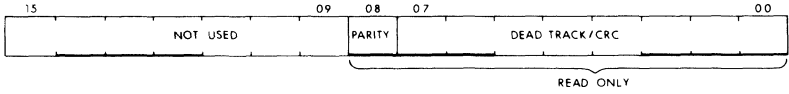
Individual bits are cleared by loading them with a 1 or by clearing ATTENTION <15> in the status register of the corresponding drive or formatter.

Also cleared by INIT.

**CHECK CHARACTER REGISTER (MTCC)**

**772460 (PDP-11)**

**Byte Offset=1C (VAX)**



**Bit            Name**

---

**15-09        NOT USED**

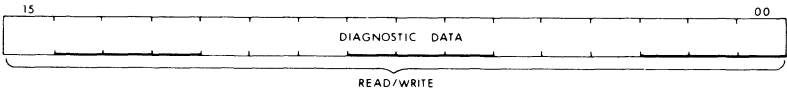
**08            DEAD TRACK PARITY/CRC PARITY**

In PE mode, this bit is set when data synchronization of the parity track is lost during a READ operation.  
 In NRZI mode, this bit is the parity bit for the CRC character.

**07-00        DEAD TRACK/CRC**

In PE mode, these bits are set to indicate the tracks that lost data synchronization during a READ operation. The formatter will perform on-the-fly data correction on one track. If more than one track of data is lost, the formatter sets INCORRECTABLE DATA ERROR <06> in the error register.  
 In NRZI mode, these bits contain the CRC character.

**DATA BUFFER REGISTER (MTDB) 772462 (PDP-11 ONLY)**



**Bit            Name**

---

**15-00        DIAGNOSTIC DATA**

This register is used for testing the controller. Up to eight words can be loaded into and read back from this register.  
 INPUT READY <06> in the control and status 2 register indicates when the register is not full and words may be loaded.  
 OUTPUT READY <07> in the control and status 2 register indicates when the register has words to be read.



## MAGNETIC TAPE REGISTERS

**Bit            Name**

---

**15            NOT SECTOR ADDRESSED**

This bit is always 0.

**14            TAPE DRIVE**

This bit is always 1.

**13            MOVING HEAD**

This bit is always 0.

**12            7 TRACK**

This bit is always 0.

**11            DRIVE REQUEST REQUIRED (DUAL-ACCESS )**

This bit is always 0.

**10            SLAVE PRESENT**

Set when the selected transport is turned on.

**09            NOT USED**

**08-06**

These bits are always 0.

**05            TM03 FORMATTER**

This bit is set when using a TM03 formatter and clear when using a TM02 formatter.

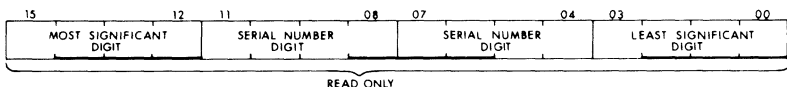
**04-00        TRANSPORT TYPE**

These bits contain  $14_8$  when the transport is a TU77,  $12_8$  when the transport is a TU45,  $11_8$  when the transport is a TE16, and  $10_8$  when the selected transport is not turned on (SLAVE PRESENT <10>).

### SERIAL NUMBER REGISTER (MTSN)

**772470 (PDP-11)**

**Byte Offset = 20 (VAX)**



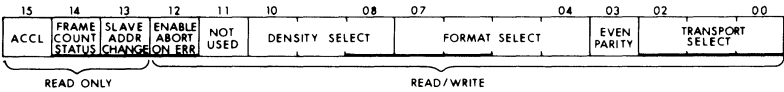
## MAGNETIC TAPE REGISTERS

This register contains the four Least Significant Digits in binary coded decimal (BCD) of the transport selected by TRANSPORT SELECT <02-00> in the tape control register.

### TAPE CONTROL REGISTER (MTTC)

**772472 (PDP-11)**

**Byte Offset = 24 (VAX)**



Bit	Name
-----	------

---

**15            ACCELERATION**

When set, indicates that the tape transport is not up to speed.

**14            FRAME COUNT STATUS**

This bit is automatically set when the frame count register is loaded. Cleared when the frame count register becomes zero.

**13            SLAVE ADDRESS CHANGE**

When set, indicates that TRANSPORT SELECT <02-00> has been changed.

Cleared when a command is executed.

**12            ENABLE ABORT ON DATA TRANSFER ERROR**

When set, a READ or WRITE operation is immediately terminated when any of the following bits in the error register is set: CORRECTABLE DATA/CRC ERROR <15>, PE FORMAT ERROR/LRC ERROR <07>, and INCORRECTABLE DATA/VERTICAL PARITY ERROR <06>.

**11            NOT USED**

**10-08        DENSITY SELECT**

These bits set the density for WRITE operations. When loaded with 011<sub>2</sub> the density is 800 b/in NRZI and when loaded with 100<sub>2</sub> the density is 1600 b/in PE.

Density can only be set when the transport is at BOT.

The formatter automatically selects density on READ operations.



## MAGNETIC TAPE REGISTERS

Bit	Name
-----	------

---

<b>15</b>	<b>ADDRESS PARITY ERROR</b>
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When set, indicates that memory has detected a parity error on the address and control lines during a data transfer.

Cleared by loading a DATA TRANSFER or FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

<b>14-11</b>	<b>NOT USED</b>
--------------	-----------------

<b>10</b>	<b>DOUBLE WORD</b>
-----------	--------------------

When set, indicates that the last memory transfer was a double word.

Cleared by loading a DATA TRANSFER or FORMATTER CLEAR command into FUNCTION CODE <05-01> in the control and status 1 register.

Also cleared by setting CONTROLLER CLEAR <05> in the control and status 2 register or INIT.

<b>9-7</b>	<b>NOT USED</b>
------------	-----------------

<b>06</b>	<b>INTERRUPT ENABLE</b>
-----------	-------------------------

Setting this bit sets INTERRUPT ENABLE <06> in the control and status 1 register.

<b>05-04</b>	<b>NOT USED</b>
--------------	-----------------

<b>03-00</b>	<b>INVERTED PARITY CHECK</b>
--------------	------------------------------

These bits are used to control the parity circuits in the controller for testing.

### TU78 REGISTERS

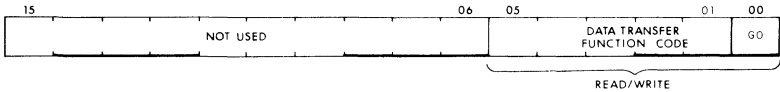
The TEU78 magnetic tape subsystems described in Chapter 3 are supported by VAX-11/780 systems only. Following are the applicable register drawings and bit definitions. Refer to the VAX Hardware Handbook for register diagrams and bit definitions for the MASSBUS adapter registers.



## MAGNETIC TAPE REGISTERS

Device registers on VAX MASSBUSes are located in a floating space starting at byte offset 400 from the base and extending to byte offset 7FC from the same base. Each of the up to eight devices supported by an MBA has a 128 byte space assigned to it. For example, the space for unit 0 would be from byte offset 400 to 47F and the space for unit 1 would be from byte offset 480 to 4FF. The byte offset bases are assigned according to the unit plug on the device. The range of byte offset bases for each of the up to eight devices supported by an MBA are as follows: 400, 480, 500, 580, 600, 680, 700, and 780. The VAX byte offsets shown here are relative to the base of the device registers.

### CONTROL REGISTER BYTE OFFSET=0



Bit	Name
-----	------

15-06	NOT USED
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05-01	DATA TRANSFER FUNCTION CODE
-------	-----------------------------

Loading these bits with one of the function codes listed below causes the formatter to perform the corresponding operation.

- |                 |  |
|-----------------|--|
| 61 <sub>8</sub> | WRITE PE<br>Writes the specified number of records and sets PE mode if tape is at BOT.           |
| 63 <sub>8</sub> | WRITE GCR<br>Writes the specified number of records and sets GCR mode if tape is at BOT.         |
| 71 <sub>8</sub> | READ   |
| 77 <sub>8</sub> | READ BACKWARD  |
| 51 <sub>8</sub> | WRITE CHECK FORWARD<br>Causes the TU78 to read forward one record and check the data for errors. |

## MAGNETIC TAPE REGISTERS

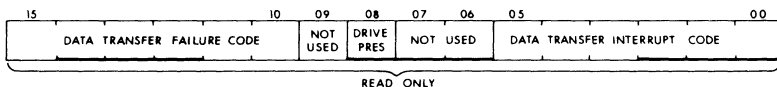
**57<sub>8</sub>**            **WRITE CHECK BACKWARD**  
Causes the TU78 to read backward one record and check the data for errors.

**73<sub>8</sub>**            **EXTENDED SENSE**  
Causes the TU78 to write 60 bytes of status information into memory.

**00**            **GO**

This bit resets at the end of each operation specified by DATA TRANSFER FUNCTION CODE <05-01>.

### DATA TRANSFER ERROR REGISTER BYTE OFFSET = 4



Bit	Name
-----	------

<b>15-10</b>	<b>DATA TRANSFER FAILURE CODE</b>
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These bits, in conjunction with the DATA TRANSFER INTERRUPT CODE <05-00>, specify data transfer status at the end of an operation.

<b>09</b>	<b>NOT USED</b>
-----------	-----------------

<b>08</b>	<b>DRIVE PRESENT</b>
-----------	----------------------

When set, indicates that the selected formatter is present and turned on.

<b>07-06</b>	<b>NOT USED</b>
--------------	-----------------

<b>05-00</b>	<b>DATA TRANSFER INTERRUPT CODE</b>
--------------	-------------------------------------

These bits, in conjunction with the DATA TRANSFER FAILURE CODE <15-10>, specify data transfer status at the end of an operation. DATA TRANSFER FAILURE and INTERRUPT CODES are as follows:

MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
01 <sub>8</sub>		<b>DONE</b> READ or WRITE operation completed successfully.
	00 <sub>8</sub>	EXTENDED SENSE data not updated.
	01 <sub>8</sub>	EXTENDED SENSE data updated.
02 <sub>8</sub>		<b>TAPE MARK</b> Tape mark detected during a READ operation.
03 <sub>8</sub>		<b>BOT</b> BOT detected during a READ BACKWARD operation.
	01 <sub>8</sub>	Command issued when tape at BOT.
	02 <sub>8</sub>	BOT detected after tape motion started.
	03 <sub>8</sub>	GCR automatic read amplification (ARA) ID burst detected.
04 <sub>8</sub>		<b>EOT</b> Tape has been moved past EOT marker.
	00 <sub>8</sub>	EXTENDED SENSE data not updated.
	01 <sub>8</sub>	EXTENDED SENSE data updated.
10 <sub>8</sub>		<b>WRITE LOCK ERROR</b> WRITE operation attempted on a file-protected tape.

MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
11 <sub>8</sub>		<b>NOT READY</b> Transport is performing a REWIND or LOAD operation.
	01 <sub>8</sub>	Transport is on-line but not ready.
	02 <sub>8</sub>	Fatal error has been detected. Operation cannot be executed until TM CLEAR <14> in the hardware control register is set.
	03 <sub>8</sub>	Transport performing a REWIND operation, executing a DATA SECURITY ERASE command from another MASSBUS, or executing a KEYPAD command.
12 <sub>8</sub>		<b>NOT AVAILABLE</b> Transport is on-line but not enabled for this MASSBUS port.
13 <sub>8</sub>		<b>OFF-LINE</b> Transport is off-line.
14 <sub>8</sub>		<b>NON-EXISTENT TRANSPORT</b> Selected transport is non-existent or is turned off.
15 <sub>8</sub>		<b>NOT CAPABLE</b> The operation cannot be performed. Reason for failure specified by the following codes:
	01 <sub>8</sub>	No data found in 25 ft of tape.
	02 <sub>8</sub>	ID burst is neither PE nor GCR.
	03 <sub>8</sub>	GCR ARA ID burst not detected.

MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
	04 <sub>8</sub>	No gap detected after PE ID burst or GCR ARA ID burst.
20 <sub>8</sub>		<b>LONG RECORD</b> The last record read was longer than the byte count.
	00 <sub>8</sub>	EXTENDED SENSE data not updated.
	01 <sub>8</sub>	EXTENDED SENSE data updated.
21 <sub>8</sub>		<b>SHORT RECORD</b> The last record read was shorter than the byte count.
	00 <sub>8</sub>	EXTENDED SENSE data not updated.
	01 <sub>8</sub>	EXTENDED SENSE data updated.
22 <sub>8</sub>		<b>RETRY</b> Data error detected and the tape positioned for retry. Operation must be repeated.
	01 <sub>8</sub>	CRC error, ACRC error, pointer mismatch, incorrectable error, or two-track error set in ECCSTA register (WRITE GCR).
	02 <sub>8</sub>	CRC error, ACRC error, or incorrectable error set in ECCSTA register (READ GCR).
	03 <sub>8</sub>	Incorrectable error set in ECCSTA register (READ PE).

## MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
	04 <sub>8</sub>	AMTIE, pointer mismatch, incor- rectable error, two-track error, or single-track error set in ECCSTA register (WRITE PE).
	05 <sub>8</sub>	At least one bit set in ECCSTA register.
	06 <sub>8</sub>	At least one write fail bit set in RPFail and RPATH registers (WRITE PE).
	07 <sub>8</sub>	More than one write fail bit set in RPFail and RPATH registers (WRITE GCR).
	10 <sub>8</sub>	RSTAT register contains bad code.
	11 <sub>8</sub>	CRC characters from WMC and RMC do not match (WRITE PE).
	12 <sub>8</sub>	MASSBUS data bus parity error.
	13 <sub>8</sub>	Record length incorrect during re- try opposite attempt. Invalid data transferred.
23 <sub>8</sub>		<b>READ OPPOSITE</b> Read error detected and the tape positioned for retry. The READ op- eration must be performed in the opposite direction.  Same as code 22 <sub>8</sub> .
24 <sub>8</sub>		<b>UNREADABLE</b> READ operation retries have failed to read the record.  Same as code 22 <sub>8</sub> .

## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
25 <sub>8</sub>		<b>ERROR</b> An error has been detected which requires a retry. SUPPRESS ERROR REPOSITIONING <15> in the tape control register is set. The tape is positioned at the beginning of the record.  Same as code 22 <sub>8</sub> .
26 <sub>8</sub>		<b>EOT ERROR</b> An error has occurred during a WRITE operation past the EOT marker. SUPPRESS ERROR REPOSITIONING <15> in the tape control register is set. The tape is positioned at the beginning of the record.  Same as code 22 <sub>8</sub> .
27 <sub>8</sub>		<b>BAD TAPE</b> Tape position has been lost or write retries have failed to write the record.  Same as code 22 <sub>8</sub> .
30 <sub>8</sub>		<b>TM FAULT A</b> Hardware has failed or software bug has been detected.
	01 <sub>8</sub>	Invalid command code.
	02 <sub>8</sub>	Data transfer command issued while a non-data transfer operation was in progress on the same transport.

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
	03 <sub>8</sub>	WMC error detected. Specified in encode register. Error may be caused by INVALID FORMAT <14-12> or SKIP COUNT <11-8> codes in the tape control register.
	04 <sub>8</sub>	Run signal not received from MBA.
	05 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (selected function routine).
	06 <sub>8</sub>	ECC ROM parity error.
	07 <sub>8</sub>	XMC ROM parity error.
	10 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ID burst during WRITE operation from BOT).
	11 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ARA burst during WRITE operation from BOT).
	12 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ARA ID burst during WRITE operation from BOT).
	13 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify Gap during WRITE operation from BOT).



## MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
	14 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Read ID burst during READ operation from BOT).
	15 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ARA ID burst during READ operation from BOT).
	16 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify Gap during READ operation from BOT).
	17 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Find Gap during ERASE GAP operation).
	20 <sub>8</sub>	WMC LEFT failed to set during EXTENDED SENSE operation.
	21 <sub>8</sub>	XL PE set in INTSTA register.
	22 <sub>8</sub>	XMC DONE did not set.
	23 <sub>8</sub>	WMC ROM PE or RD PE set in WMCERR register.
31 <sub>8</sub>		<b>TU FAULT A</b> Transport has failed.
	01 <sub>8</sub>	TU Status parity error.
	02 <sub>8</sub>	TU Command parity error.

## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
	03 <sub>8</sub>	Transport went off-line during REWIND operation.
	04 <sub>8</sub>	Transport became ready during DATA SECURITY ERASE operation.
	05 <sub>8</sub>	TU CMD status changed during DATA SECURITY ERASE operation.
	06 <sub>8</sub>	Transport velocity never came up to speed.
	07 <sub>8</sub>	Transport velocity changed after it was up to speed and a WRITE operation started.
	10 <sub>8</sub>	TU CMD did not load correctly to start tape motion in the selected function routine.
	11 <sub>8</sub>	TU CMD did not load correctly to set drive density.
	12 <sub>8</sub>	TU CMD did not load correctly to start tape motion to write BOT ID burst.
	13 <sub>8</sub>	TU CMD did not load correctly to backup tape to BOT after failing to write BOT ID burst.
	14 <sub>8</sub>	Failed to write density ID burst correctly.
	15 <sub>8</sub>	Failed to write ARA burst correctly.
	16 <sub>8</sub>	Failed to write ARA ID burst correctly.

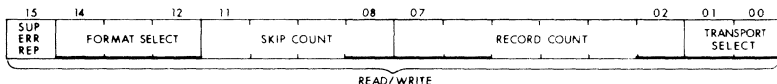
## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
	17 <sub>8</sub>	ARA error bit set in MTA status B register.
	21 <sub>8</sub>	Gap after correct ID burst not detected during a WRITE operation.
	22 <sub>8</sub>	TU CMD did not load correctly to start tape motion to read ID burst.
	23 <sub>8</sub>	Time-out looking for BOT after detecting ARA ID burst.
	24 <sub>8</sub>	Failed to write tape mark correctly.
	25 <sub>8</sub>	Tape never came up to speed while trying to reposition for retry of WRITE TAPE MARK.
	26 <sub>8</sub>	TU CMD did not load correctly to start tape motion in Erase Gap routine.
	27 <sub>8</sub>	Gap in Erase Gap routine not detected.
	30 <sub>8</sub>	Gap after a WRITE operation not detected.
	31 <sub>8</sub>	Read path terminated before entire record was written.
	32 <sub>8</sub>	Gap after a WRITE operation not detected and read path terminated early.
	33 <sub>8</sub>	TU CMD did not load correctly to backup for retry of WRITE TAPE MARK.

MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
	34 <sub>8</sub>	Transport velocity changed after it was up to speed while trying to re-position for retry of WRITE TAPE MARK.
	35 <sub>8</sub>	TU CMD did not load correctly to backup to retry reading BOT ID burst.
	36 <sub>8</sub>	Time-out looking for BOT after failing to write BOT ID burst.
	37 <sub>8</sub>	Transport velocity changed while writing PE gap before starting to write record.
	40 <sub>8</sub>	TU CMD did not load correctly to set PE tape density at start of write BOT ID burst.
	41 <sub>8</sub>	TU CMD did not load correctly to set GCR tape density after writing Density ID burst.
	42 <sub>8</sub>	TU CMD did not load correctly to set PE tape density at start of READ operation from BOT.
	43 <sub>8</sub>	TU CMD did not load correctly to set GCR tape density after reading a GCR Density ID burst.

TAPE CONTROL REGISTER BYTE OFFSET=8



## MAGNETIC TAPE REGISTERS

**Bit**            **Name**

**15**            **SUPPRESS ERROR REPOSITIONING**

When set, prevents the TU78 from backing the tape up to the beginning of the record when it detects a data error.

**14-12**        **FORMAT SELECT**

These bits specify the method by which 8-bit bytes will be packed into or unpacked from 16-bit words during DATA TRANSFER operations. Code 000<sub>2</sub> selects Normal mode and code 001<sub>2</sub> selects Reversed mode

**11-08**        **SKIP COUNT**

During a READ operation, these bits specify the number of bytes to be loaded with zeros before the first byte of data is read from the tape.

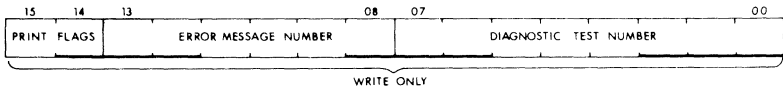
**07-02**        **RECORD COUNT**

These bits specify the number of records to be read into or written from the tape.

**01-00**        **TRANSPORT SELECT**

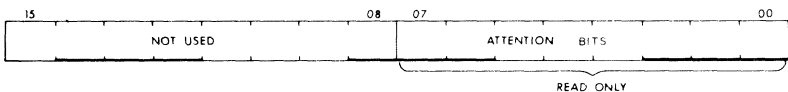
These bits specify the address of the transport that is to perform the DATA TRANSFER operation.

### REGISTER 3 BYTE OFFSET = C



This register is used for diagnostic testing.

### ATTENTION SUMMARY REGISTER BYTE OFFSET = 10



# MAGNETIC TAPE REGISTERS

**Bit**            **Name**

---

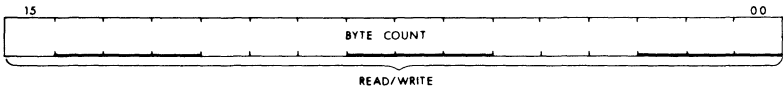
**15-08**        **NOT USED**

**07-00**        **ATTENTION BITS**

On VAX systems that mix tape transports and disk drives on the same MBA, these bits correspond to ATTENTION <15> in the status registers for disk drives 7-0 or the tape formatter.

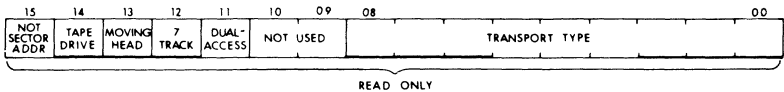
Individual bits are cleared by loading them with a 1 or by clearing ATTENTION <15> in the status register of the corresponding drive or formatter.

## BYTE COUNT REGISTER BYTE OFFSET = 14



This register specifies the number of bytes to be written in each record or the number of bytes to be read. Even if the record read is longer than the byte count, all of the data bytes are sent to the MBA. After the operation the byte count register will contain the actual number of bytes in the record.

## DRIVE TYPE REGISTER BYTE OFFSET = 18



**Bit**            **Name**

---

**15**            **NOT SECTOR ADDRESSED**

This bit is always 0.

**14**            **TAPE DRIVE**

This bit is always 1.

## MAGNETIC TAPE REGISTERS

### 13 MOVING HEAD

This bit is always 0.

### 12 7 TRACK

This bit is always 0.

### 11 DUAL-ACCESS

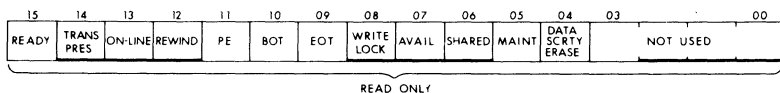
When set, indicates that the dual MASSBUS port option has been installed.

### 10-09 NOT USED

### 08-00 TRANSPORT TYPE

These bits are equal to  $101_8$ .

## STATUS REGISTER BYTE OFFSET=1C



Bit	Name
-----	------

15	READY
----	-------

When set, indicates that the selected transport is on-line and ready to perform an operation.

14	TRANSPORT PRESENT
----	-------------------

When set, indicates that the selected transport is turned on.

13	ON-LINE
----	---------

When set, indicates that the selected transport is on-line.

12	REWIND
----	--------

When set, indicates that the selected transport is rewinding.

## MAGNETIC TAPE REGISTERS

### 11 PE

When set, indicates that the selected transport is set to operate in PE mode.

When clear, indicates that the selected transport is set to operate in GCR mode.

### 10 BOT

When set, indicates that the selected transport is at BOT.

### 09 EOT

When set, indicates that the selected transport has passed the EOT marker.

### 08 WRITE LOCKED

When set, indicates that the tape reel on the selected transport does not have a file-protect ring, i.e. the transport is write-protected.

### 07 AVAILABLE

When set, indicates that the selected transport is available to this MASSBUS port.

### 06 SHARED

When set, indicates that the selected transport is available to both MASSBUS ports.

### 05 MAINTENANCE

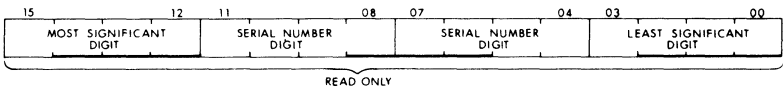
When set, indicates that the selected transport is in Maintenance mode and cannot be used.

### 04 DATA SECURITY ERASE

When set, indicates that the selected transport is performing a DATA SECURITY ERASE operation.

### 03-00 NOT USED

## SERIAL NUMBER REGISTER BYTE OFFSET = 20

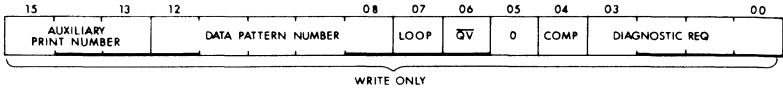




## MAGNETIC TAPE REGISTERS

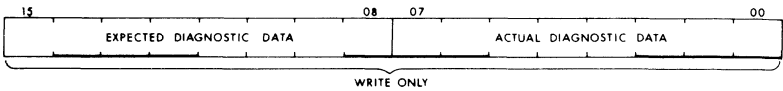
This register contains the four Least Significant Digits in binary coded decimal (BCD) of the selected transport.

### REGISTER 11 BYTE OFFSET=24



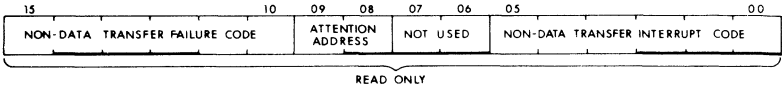
This register is used for diagnostic testing.

### REGISTER 12 BYTE OFFSET=28



This register is used for diagnostic testing.

### NON-DATA TRANSFER ERROR REGISTER BYTE OFFSET=2C



**Bit**            **Name**

**15-10**            **NON-DATA TRANSFER FAILURE CODE**

These bits, in conjunction with the NON-DATA TRANSFER INTERRUPT CODE <05-00>, specify data transfer status at the end of an operation.

**09-08**            **ATTENTION ADDRESS**

These bits specify the transport that generated the interrupt.

**07-06**            **NOT USED**

**05-00**            **NON-DATA TRANSFER INTERRUPT CODE**

These bits, in conjunction with the NON-DATA TRANSFER FAILURE

## MAGNETIC TAPE REGISTERS

CODE <15-10>, specify non-data transfer status at the end of an operation. NON-DATA TRANSFER FAILURE and INTERRUPT CODES are as follows:

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
01 <sub>8</sub>		<b>DONE</b> Operation completed successfully.
	00 <sub>8</sub>	EXTENDED SENSE data not updated.
	01 <sub>8</sub>	EXTENDED SENSE data updated.
02 <sub>8</sub>		<b>TAPE MARK</b> Tape mark detected.
03 <sub>8</sub>		<b>BOT</b> BOT detected during a backward operation.
	01 <sub>8</sub>	Command issued when tape at BOT.
	02 <sub>8</sub>	BOT detected after tape motion started.
	03 <sub>8</sub>	GCR automatic read amplification (ARA) ID burst detected.
04 <sub>8</sub>		<b>EOT</b> Tape has been moved past the EOT marker.
	00 <sub>8</sub>	EXTENDED SENSE data not updated.
	01 <sub>8</sub>	EXTENDED SENSE data updated.
05 <sub>8</sub>		<b>LOGICAL END OF TAPE</b> Two tape marks in a row have been detected.

## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
06 <sub>8</sub>		<b>NO OP</b> A NO OPERATION command has been executed.
07 <sub>8</sub>		<b>REWIND</b> The transport has started a REWIND operation.
10 <sub>8</sub>		<b>WRITE LOCK ERROR</b> A WRITE TAPE MARK, ERASE GAP, or DATA SECURITY ERASE operation has been attempted on a file-protected tape.
11 <sub>8</sub>		<b>NOT READY</b> Transport is performing a REWIND or LOAD operation or a DATA SECURITY ERASE operation from the other MASSBUS port.
	01 <sub>8</sub>	Transport is on-line but not ready.
	02 <sub>8</sub>	Fatal error has been detected. Operation cannot be executed until TM CLEAR <14> in the hardware control register is set.
	03 <sub>8</sub>	Transport performing a REWIND operation, executing a DATA SECURITY ERASE command from another MASSBUS, or executing a KEYPAD command.
12 <sub>8</sub>		<b>NOT AVAILABLE</b> Transport is on-line but not enabled for this MASSBUS port.
13 <sub>8</sub>		<b>OFF-LINE</b> Transport is off-line.

MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
14 <sub>8</sub>		<b>NON-EXISTENT TRANSPORT</b> Transport is non-existent or turned off.
15 <sub>8</sub>		<b>NOT CAPABLE</b> The operation cannot be performed. Reason for failure specified by the following codes:
	01 <sub>8</sub>	No data found in 25 ft of tape.
	02 <sub>8</sub>	ID burst is neither PE nor GCR.
	03 <sub>8</sub>	GCR ARA ID burst not detected.
	04 <sub>8</sub>	No gap detected after PE ID burst or GCR ARA ID burst.
27 <sub>8</sub>		<b>BAD TAPE</b> Tape position has been lost.
	01 <sub>8</sub>	CRC error, ACRC error, pointer mismatch, incorrectable error, or two-track error set in ECCSTA register (WRITE GCR).
	02 <sub>8</sub>	CRC error, ACRC error, or incorrectable error set in ECCSTA register (READ GCR).
	03 <sub>8</sub>	Incorrectable error set in ECCSTA register (READ PE).
	04 <sub>8</sub>	AMTIE, pointer mismatch, incorrectable error, two-track error, or single-track error set in ECCSTA register (WRITE PE).
	05 <sub>8</sub>	At least one bit set in ECCSTA register.

MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
	06 <sub>8</sub>	At least one write fail bit set in RPFAIL and RPATH registers (WRITE PE).
	07 <sub>8</sub>	More than one write fail bit set in RPFAIL and RPATH registers (WRITE GCR).
	10 <sub>8</sub>	RSTAT register contains bad code.
	11 <sub>8</sub>	CRC characters from WMC and RMC do not match (WRITE PE).
	12 <sub>8</sub>	MASSBUS data bus parity error.
	13 <sub>8</sub>	Record length incorrect during re-try opposite attempt. Invalid data transferred.
30 <sub>8</sub>		<b>TM FAULT A</b> Hardware has failed or software bug has been detected.
	01 <sub>8</sub>	Invalid command code.
	02 <sub>8</sub>	Data transfer command issued while a non-data transfer operation was in progress on the same transport.
	03 <sub>8</sub>	WMC error detected. Specified in encode register. Error may be caused by INVALID FORMAT <14-12> or SKIP COUNT <11-8> codes in the tape control register.
	04 <sub>8</sub>	Run signal not received from MBA.
	05 <sub>8</sub>	Command read from RMC register.

## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
		RCMLP did not match command loaded into RCMD register (selected function routine).
	06 <sub>8</sub>	ECC ROM parity error.
	07 <sub>8</sub>	XMC ROM parity error.
	10 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ID burst during WRITE operation from BOT).
	11 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ARA burst during WRITE operation from BOT).
	12 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify ARA ID burst during WRITE operation from BOT).
	13 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify Gap during WRITE operation from BOT).
	14 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Read ID burst during READ operation from BOT).
	15 <sub>8</sub>	Command read from RMC register. RCMLP did not match

## MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
		command loaded into RCMD register (Verify ARA ID burst during READ operation from BOT).
	16 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Verify Gap during READ operation from BOT).
	17 <sub>8</sub>	Command read from RMC register. RCMLP did not match command loaded into RCMD register (Find Gap during ERASE GAP operation).
	20 <sub>8</sub>	WMC LEFT failed to set during EXTENDED SENSE operation.
	21 <sub>8</sub>	XL PE set in INTSTA register.
	22 <sub>8</sub>	XMC DONE did not set.
	23 <sub>8</sub>	WMC ROM PE or RD PE set in WMCERR register.
31 <sub>8</sub>		<b>TU FAULT A</b> Transport has failed.
	01 <sub>8</sub>	TU Status parity error.
	02 <sub>8</sub>	TU Command parity error.
	03 <sub>8</sub>	Transport went off-line during REWIND operation.
	04 <sub>8</sub>	Transport became ready during DATA SECURITY ERASE operation.

## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
	05 <sub>8</sub>	TU CMD status changed during DATA SECURITY ERASE operation.
	06 <sub>8</sub>	Transport velocity never came up to speed.
	07 <sub>8</sub>	Transport velocity changed after it was up to speed and a WRITE operation started.
	10 <sub>8</sub>	TU CMD did not load correctly to start tape motion in the selected function routine.
	11 <sub>8</sub>	TU CMD did not load correctly to set drive density.
	12 <sub>8</sub>	TU CMD did not load correctly to start tape motion to write BOT ID burst.
	13 <sub>8</sub>	TU CMD did not load correctly to backup tape to BOT after failing to write BOT ID burst.
	14 <sub>8</sub>	Failed to write density ID burst correctly.
	15 <sub>8</sub>	Failed to write ARA burst correctly.
	16 <sub>8</sub>	Failed to write ARA ID burst correctly.
	17 <sub>8</sub>	ARA error bit set in MTA status B register.
	21 <sub>8</sub>	Gap after correct ID burst not detected during a WRITE operation.



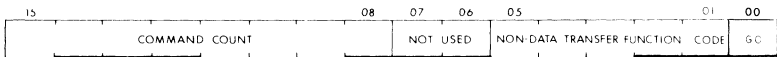
## MAGNETIC TAPE REGISTERS

<b>INTER- RUPT CODE</b>	<b>FAILURE CODE</b>	<b>DESCRIPTION</b>
	22 <sub>8</sub>	TU CMD did not load correctly to start tape motion to read ID burst.
	23 <sub>8</sub>	Time-out looking for BOT after detecting ARA ID burst.
	24 <sub>8</sub>	Failed to write tape mark correctly.
	25 <sub>8</sub>	Tape never came up to speed while trying to reposition for retry of WRITE TAPE MARK.
	26 <sub>8</sub>	TU CMD did not load correctly to start tape motion in Erase Gap routine.
	27 <sub>8</sub>	Gap in Erase Gap routine not detected.
	30 <sub>8</sub>	Gap after a WRITE operation not detected.
	31 <sub>8</sub>	Read path terminated before entire record was written.
	32 <sub>8</sub>	Gap after a WRITE operation not detected and read path terminated early.
	33 <sub>8</sub>	TU CMD did not load correctly to backup for retry of WRITE TAPE MARK.
	34 <sub>8</sub>	Transport velocity changed after it was up to speed while trying to reposition for retry of WRITE TAPE MARK.
	35 <sub>8</sub>	TU CMD did not load correctly to

## MAGNETIC TAPE REGISTERS

INTER- RUPT CODE	FAILURE CODE	DESCRIPTION
		backup to retry reading BOT ID burst.
	36 <sub>8</sub>	Time-out looking for BOT after failing to write BOT ID burst.
	37 <sub>8</sub>	Transport velocity changed while writing PE gap before starting to write record.
	40 <sub>8</sub>	TU CMD did not load correctly to set PE tape density at start of write BOT ID burst.
	41 <sub>8</sub>	TU CMD did not load correctly to set GCR tape density after writing Density ID burst.
	42 <sub>8</sub>	TU CMD did not load correctly to set PE tape density at start of READ operation from BOT.
	43 <sub>8</sub>	TU CMD did not load correctly to set GCR tape density after reading a GCR Density ID burst. <sup>v</sup>

### NON-DATA TRANSFER CONTROL REGISTER BYTE OFFSET = 30



Bit	Name
-----	------

<b>15-08</b>	<b>COMMAND COUNT</b>
--------------	----------------------

These bits specify the number of times the operation corresponding to the code loaded into NON-DATA TRANSFER FUNCTION CODE <05-01 > is to be performed on transport 0.

## MAGNETIC TAPE REGISTERS

**07-06 NOT USED**

**05-01 NON-DATA TRANSFER FUNCTION CODE**

Loading these bits with one of the function codes listed below causes the formatter to perform the corresponding operation on transport 0.

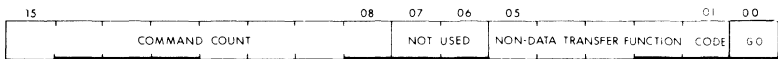
- |                 |   |
|-----------------|---|
| 07 <sub>8</sub> | <b>REWIND</b><br>Causes the tape transport to rewind to BOT.  |
| 05 <sub>8</sub> | <b>UNLOAD</b><br>Causes the tape transport to rewind to BOT and unload the tape.                                    |
| 15 <sub>8</sub> | <b>WRITE TAPE MARK PE</b><br>Writes a tape mark.<br>Sets PE mode if tape is at BOT.                                 |
| 17 <sub>8</sub> | <b>WRITE TAPE MARK GCR</b><br>Writes a tape mark.<br>Sets GCR mode if tape is at BOT.                               |
| 41 <sub>8</sub> | <b>CLOSE FILE PE</b><br>Writes two tape marks and then backs up one tape mark.<br>Sets PE mode if tape is at BOT.   |
| 43 <sub>8</sub> | <b>CLOSE FILE GCR</b><br>Writes two tape marks and then backs up one tape mark.<br>Sets GCR mode if tape is at BOT. |
| 35 <sub>8</sub> | <b>ERASE GAP PE</b><br>Erases 3.2 in of tape.<br>Sets PE mode if tape is at BOT.                                    |
| 37 <sub>8</sub> | <b>ERASE GAP GCR</b><br>Erases 3.2 in of tape.<br>Sets GCR mode if tape is at BOT.                                  |
| 21 <sub>8</sub> | <b>SPACE BLOCKS FORWARD</b><br>Spaces forward the specified number of blocks.<br>Tape marks are ignored.            |

## MAGNETIC TAPE REGISTERS

23 <sub>8</sub>	<b>SPACE BLOCKS BACKWARD</b> Spaces backward the specified number of blocks. Tape marks are ignored.
25 <sub>8</sub>	<b>SPACE FILES FORWARD</b> Spaces forward the specified number of files.
47 <sub>8</sub>	<b>SPACE FILES FORWARD/STOP IF LOGICAL EOT</b> Spaces forward the specified number of files but stops if two tape marks in a row are detected.
27 <sub>8</sub>	<b>SPACE FILES BACKWARD</b> Spaces backward the specified number of files.
45 <sub>8</sub>	<b>SPACE TO LOGICAL EOT</b> Spaces forward until two tape marks in a row are detected and then backs up one tape mark.
31 <sub>8</sub>	<b>SPACE FORWARD EITHER</b> Spaces forward the specified number of blocks and counts tape marks as blocks.
33 <sub>8</sub>	<b>SPACE BACKWARD EITHER</b> Spaces backward the specified number of blocks and counts tape marks as blocks.
13 <sub>8</sub>	<b>DATA SECURITY ERASE</b> Erases the remainder of the tape to 10 ft past the EOT marker and then rewinds the tape.
11 <sub>8</sub>	<b>SENSE</b> Causes the formatter to update the status information in the registers.
03 <sub>8</sub>	<b>NO OPERATION</b>
00	<b>GO</b>

This bit resets at the end of each operation specified by FUNCTION CODE <05-01 > .

**NON-DATA TRANSFER CONTROL REGISTER BYTE OFFSET=34**



**Bit Name**

---

**15-08 COMMAND COUNT**

These bits specify the number of times the operation corresponding to the code loaded into NON-DATA TRANSFER FUNCTION CODE <05-01> is to be performed on transport 1.

**07-06 NOT USED**

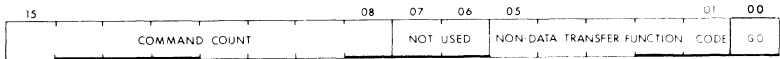
**05-01 NON-DATA TRANSFER FUNCTION CODE**

Loading these bits with one of the function codes listed under the Non-Data Transfer Control Register for transport 0 causes the formatter to perform the corresponding operation on transport 1.

**00 GO**

This bit resets at the end of each operation specified by FUNCTION CODE <05-01> .

**NON-DATA TRANSFER CONTROL REGISTER BYTE OFFSET=38**



**Bit Name**

---

**15-08 COMMAND COUNT**

These bits specify the number of times the operation corresponding to the code loaded into NON-DATA TRANSFER FUNCTION CODE <05-01> is to be performed on transport 2.

**07-06 NOT USED**

**05-01 NON-DATA TRANSFER FUNCTION CODE**

Loading these bits with one of the function codes listed under the Non-

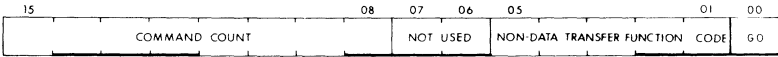
## MAGNETIC TAPE REGISTERS

Data Transfer Control Register for transport 0 causes the formatter to perform the corresponding operation on transport 2.

**00 GO**

This bit resets at the end of each operation specified by FUNCTION CODE <05-01> .

### NON-DATA TRANSFER CONTROL REGISTER BYTE OFFSET=3C



**Bit Name**

**15-08 COMMAND COUNT**

These bits specify the number of times the operation corresponding to the code loaded into NON-DATA TRANSFER FUNCTION CODE <05-01> is to be performed on transport 3.

**07-06 NOT USED**

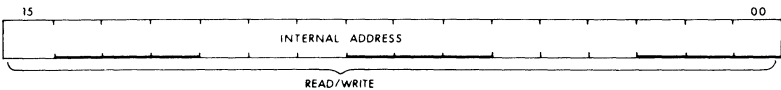
**05-01 NON-DATA TRANSFER FUNCTION CODE**

Loading these bits with one of the function codes listed under the Non-Data Transfer Control Register for transport 0 causes the formatter to perform the corresponding operation on transport 3.

**00 GO**

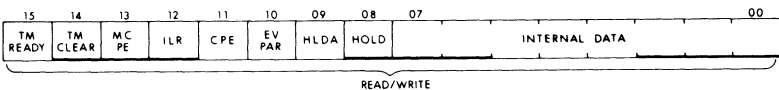
This bit resets at the end of each operation specified by FUNCTION CODE <05-01> .

### HARDWARE CONTROL REGISTER 0 BYTE OFFSET=40



This register is used for diagnostic testing.

### HARDWARE CONTROL REGISTER 1 BYTE OFFSET=44



This register is used for diagnostic testing.

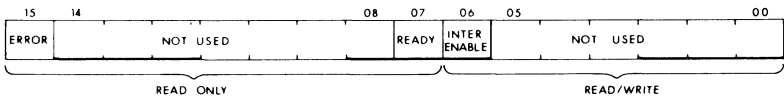
## LINEPRINTER REGISTERS

### LINEPRINTER REGISTERS

#### LXY11/LXY21 SERIES REGISTERS

The LXY11/LXY21 printer/plotter systems described in Chapter 4 use the same controller. Following are the register drawings and bit definitions of the controller's two registers: the Control and Status Register and the Data Buffer Register.

#### CONTROL AND STATUS REGISTER (LXCS) 777514



Bit	Name
-----	------

15	ERROR
----	-------

Set whenever an error condition exists in the printer/plotter. Error conditions are power off, printer/plotter off-line, no paper, torn paper, or form thickness adjustment lever left up. Generates an interrupt if INTERRUPT ENABLE <06> is also set. Cleared by correcting the error condition.

14-08	NOT USED
-------	----------

07	READY
----	-------

Set when the printer/plotter is ready for the next character to be loaded into the data buffer register. Generates an interrupt if INTERRUPT ENABLE <06> is also set.

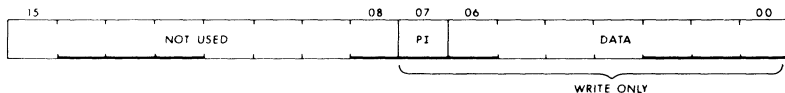
06	INTERRUPT ENABLE
----	------------------

When set allows an interrupt to occur when either the ERROR <15> or READY <07> bit is also set. Cleared by loading with a 0. Also cleared by INIT.

05-00	NOT USED
-------	----------

## LINEPRINTER REGISTERS

### DATA BUFFER REGISTER (LXDB) 777516



Bit	Name
-----	------

15-08	NOT USED
-------	----------

07	PAPER INSTRUCTION (PI)
----	------------------------

Used to advance the paper up to 15 lines when data bit <04> is also set. Data bits <03-00> contain the number of lines to be advanced. NOTE: When the PLXY-11 plot software is used with some operating systems the PI is disabled by installing jumper W5 on the controller logic board "A".

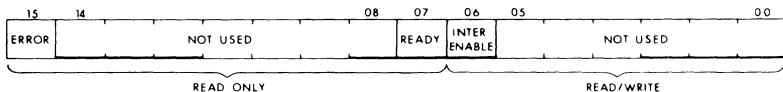
06-00	DATA
-------	------

7-bit ASCII character buffer. Characters are transferred to the li-  
neprinter by loading this buffer.

### LP11 SERIES REGISTERS

The LP11 lineprinter systems described in Chapter 4 use the same controller. Following are the register drawings and bit definitions of the controller's two registers: the Control and Status Register and the Data Buffer Register.

### CONTROL AND STATUS REGISTER (LPCS) 777514





## LINEPRINTER REGISTERS

**Bit            Name**

---

**15            ERROR**

Set when an error condition exists in the lineprinter. Error conditions are power off, no paper, torn paper, lineprinter drum gate or band gate open, over-temperature alarm, or lineprinter off-line.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

Cleared by correcting the error condition.

**14-08        NOT USED**

**07            READY**

Set when the lineprinter is ready for the next character to be loaded into the data buffer register.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

**06            INTERRUPT ENABLE**

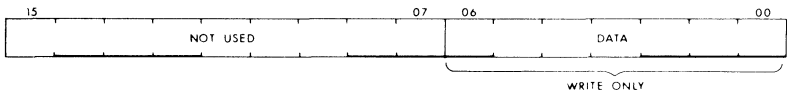
When set allows an interrupt to occur when either the ERROR <15> or READY <07> bit is also set.

Cleared by loading with a 0.

Also cleared by INIT.

**05-00        NOT USED**

### DATA BUFFER REGISTER (LPDB) 777516



**15-07        NOT USED**

**06-00        DATA**

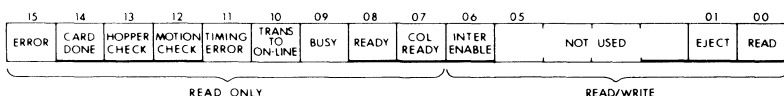
7-bit ASCII character buffer. Characters are transferred to the lineprinter by loading this buffer.

## CARD READER REGISTERS

### CR11 & CME11/CMS11 SERIES REGISTERS

The CR11 and CMS11/CME11 card reader systems described in Chapter 5 use the same controller. Following are the register drawings and bit definitions of the controller's four registers: the Status Register, the two Data Buffer Registers, and the Maintenance Register.

### STATUS REGISTER (CRS) 777160



Bit	Name
-----	------

15	<b>ERROR</b>
----	--------------

Set by card reader going off-line (READY <08>) or set by TIMING ERROR <11>.

Generates an interrupt if the INTERRUPT ENABLE <06> bit is also set.

When set, ignores READ commands.

Cleared by loading status register bits <00-06> when the error has been corrected.

Also cleared by INIT.

14	<b>CARD DONE</b>
----	------------------

When set, indicates that the card reader has finished reading a card and is ready to accept another READ <00> command.

Clears READ <00> bit.

Generates an interrupt if the INTERRUPT ENABLE <06> bit is also set.

Cleared by loading status register bits <00-06>.

Also cleared by INIT.

13	<b>HOPPER CHECK</b>
----	---------------------

When set, indicates that either the input hopper is empty or that the output stacker is full.

## CARD READER REGISTERS

Causes the card reader to go off-line and sets the READER READY STATUS <08> bit.

Cleared by correcting the error condition.

### 12 MOTION CHECK

When set, indicates either of the following error conditions: the card reader feed mechanism failed to feed a card into the reader station when requested (PICK CHECK) or a card was not delivered to the output stacker indicating a card jam (STACK CHECK).

Causes the card reader to go off-line and sets the READER READY STATUS <08> bit.

Cleared by correcting the error condition.

### 11 TIMING ERROR

When set, indicates that a new card column of data has been loaded into the data buffer register before a previously loaded column was read by the program and sets the ERROR <15> bit.

Cleared by loading status register bits <00-06>.

Also cleared by INIT.

### 10 READER TRANSITION TO ON-LINE

When set, this bit indicates that the card reader has gone on-line and now is under program control.

Generates an interrupt if the INTERRUPT ENABLE <06> bit is also set.

Cleared by loading status register bits <00-06>.

Also cleared by INIT.

### 09 BUSY

When set, indicates that a card is in the process of being read.

Cleared when card has been read (CARD DONE <14>).

### 08 READER READY STATUS

When set, this bit indicates that the card reader is off-line and sets the ERROR <15> bit.

Set by HOPPER CHECK <13> or MOTION CHECK <12>.

Cleared by operator intervention.

When clear, indicates the card reader is on-line and ready to accept a READ command.

### 07 COLUMN READY

When set, indicates that one column of data has been loaded into the

## CARD READER REGISTERS

data buffer register and is ready for transfer to the UNIBUS.

Cleared by reading either of the controller data buffer registers (CRB1 or CRB2).

Also cleared by INIT.

### 06 INTERRUPT ENABLE

When set, allows an interrupt to occur if one of the following bits is also set: CARD DONE <14>, READER TRANSITION TO ON-LINE <10>, COLUMN READY <07>, or ERROR <15>.

Cleared by loading with a 0.

Also cleared by INIT.

### 05-02 NOT USED

### 01 EJECT

When set, causes the remaining columns of a card to be skipped by inhibiting COLUMN READY <07>, although data transfers from the card reader to the data buffer registers still take place.

TIMING ERROR <11> can occur if the data that was in the data buffer register when the EJECT bit was set is not read.

When set and followed by a READ command, causes an entire card to be skipped.

Cleared by INIT.

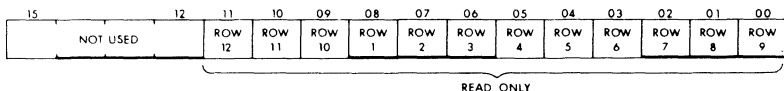
### 00 READ

When set, this bit causes the card reader feed mechanism to feed a card into the read station.

Cleared by CARD DONE <14>.

Also cleared by INIT.

## DATA BUFFER REGISTER (CRB1) 777162



Bit	Name
-----	------

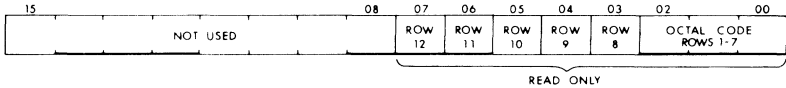
15-12	NOT USED
-------	----------

## CARD READER REGISTERS

### 11-00 DATA

These bits contain a 12-bit data character read directly from rows 1-12 of the card column.

### DATA BUFFER REGISTER (CRB2) 777164



**Bit Name**

**15-08 NOT USED**

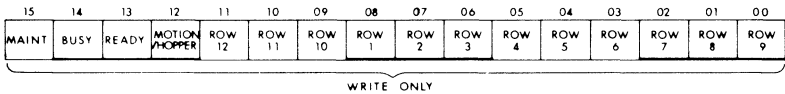
**07-03 DATA**

Data read directly from rows 8-12 of card column.

**02-00 3-BIT OCTAL CODE**

Encoded 3-bit octal representation of rows 1-7.

### MAINTENANCE REGISTER (CRM) 777166



**NOTE:** This register is used to perform diagnostics on the card reader controller. The card reader need not be connected to the controller.

**Bit Name**

**15 MAINTENANCE**

When set, enables the functions of bits <14-12> and the transfer of diagnostic data from bits <11-00> to data buffer register, CRB1.

**14 BUSY**

When set and the MAINTENANCE <15> bit is also set, sets the BUSY <09> bit in the controller status register.

**13 READY**

When set and the MAINTENANCE <15> bit is also set, sets the READER READY STATUS <08> bit in the controller status register.

**12 MOTION/HOPPER**

When set and the MAINTENANCE <15> bit is also set, sets the HOPPER CHECK <13> bit and the MOTION CHECK <12> bit in the controller status register.

**11-00 DIAGNOSTIC DATA**

When the MAINTENANCE <15> bit is set, bits <00-11> are loaded into the data buffer register, CRB1.

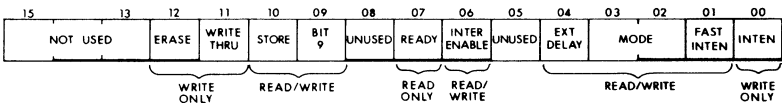
**SENSOR I/O DEVICE REGISTERS**

**AA11-K REGISTERS**

The AA11-K digital-to-analog converter described in Chapter 6 has five registers: the Display Status Register and four Data Buffer Registers. Following are the register drawings and bit definitions of the AA11-K registers.

The AA11-K has a floating address which allows the use of more than one AA11-K on a system and avoids address conflicts with other options.

**DISPLAY STATUS REGISTER (DSR) 770416**



**Bit Name**

**15-13 NOT USED**

## SENSOR I/O DEVICE REGISTERS

### 12 ERASE

When set, this bit sets the erase line to the oscilloscope causing it to erase the screen.

### 11 WRITE THRU

When set, this bit sets the write thru line to the oscilloscope inhibiting dot or intensified point positions from being stored on the screen even though the user is doing a STORE operation.

### 10 STORE

When set, this bit sets the store line to the oscilloscope causing it to store all subsequent dot positions until cleared. It also increases the INTENSIFY pulse width from 2  $\mu$ s to 6  $\mu$ s.

### 09 BIT 9

When set, this bit sets the bit 9 line in the I/O connector.

### 08 NOT USED

### 07 READY

Set after the INTENSIFY pulse is sent to the oscilloscope or when the oscilloscope sets the erase return line indicating that an erase operation is complete.

When set, indicates that the oscilloscope is ready for new data to be loaded into the data buffer registers and sets the ready line to the oscilloscope unless EXTERNAL DELAY <04> is also set.

Generates an interrupt if INTERRUPT ENABLE <06> is also set.

### 06 INTERRUPT ENABLE

When set, generates an interrupt if READY <07> is also set.

### 05 NOT USED

### 04 EXTERNAL DELAY

When this bit is equal to 1, all internal timing stops and the READY signal at the I/O connector goes low. When the external device (oscilloscope or X/Y recorder) returns a DELAY RET signal, an INTENSIFY pulse will be generated and READY <07> will be set.

## SENSOR I/O DEVICE REGISTERS

### 03-02      **MODE**

Loading these bits selects the mode in which the AA11-K will generate the INTENSIFY pulse.

00<sub>2</sub> The INTENSIFY pulse is sent to the oscilloscope when INTENSIFY <00> is set.

01<sub>2</sub> X MODE The INTENSIFY pulse is generated by loading Data Buffer Register, Channel 0 (X-DAC0).

10<sub>2</sub> Y MODE The INTENSIFY pulse is generated by loading Data Buffer Register, Channel 1 (Y-DAC1).

11<sub>2</sub> XY MODE The INTENSIFY pulse is generated by loading either Data Buffer Register, Channel 0 (X-DAC0) or Data Buffer Register, Channel 1 (Y-DAC1).

### 01            **FAST INTENSIFY**

When set, changes the settling delay to 3  $\mu$ s. When cleared, the settling delay is returned to 20  $\mu$ s or 80  $\mu$ s (jumper-selectable).

### 00            **INTENSIFY**

When set, sends an INTENSIFY pulse to the oscilloscope on the intensify line if MODE <03-02> is set to 00<sub>2</sub>.

### **DATA BUFFER REGISTER, CHANNEL 0 (X-DAC0) 770420**



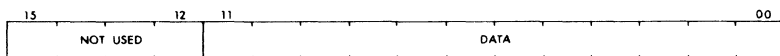
Bit	Name
-----	------

15-12	NOT USED
-------	----------

11-00	DATA
-------	------

12 bits of data to be converted to an analog voltage.

### **DATA BUFFER REGISTER, CHANNEL 1 (Y-DAC1) 770422**



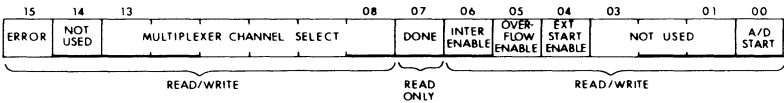




## SENSOR I/O DEVICE REGISTERS

register drawings and bit definitions of the AD11-K registers. The AD11-K has a floating address which allows the use of more than one AD11-K on a system and avoids address conflicts with other options.

### STATUS REGISTER 1704000



Bit	Name
-----	------

<b>15</b>	<b>ERROR</b>
-----------	--------------

When set, indicates that a second A/D conversion has ended before data from the previous A/D conversion has been read or that a second A/D conversion has been initiated before the first conversion has been completed.

<b>14</b>	<b>NOT USED</b>
-----------	-----------------

<b>13-08</b>	<b>MULTIPLEXER (MUX) CHANNEL SELECT</b>
--------------	---

These bits define which A/D input channel is to be sampled.

<b>07</b>	<b>DONE</b>
-----------	-------------

When set, indicates the completion of an A/D conversion. Generates an interrupt if INTERRUPT ENABLE <06> is set. Cleared when the interrupt is serviced or when the buffer register is read.

<b>06</b>	<b>INTERRUPT ENABLE</b>
-----------	-------------------------

When set, causes an interrupt if DONE <07> is also set.

<b>05</b>	<b>OVERFLOW ENABLE</b>
-----------	------------------------

When set, overflow from a KW11-K realtime clock initiates A/D conversion.

<b>04</b>	<b>EXTERNAL START ENABLE</b>
-----------	------------------------------

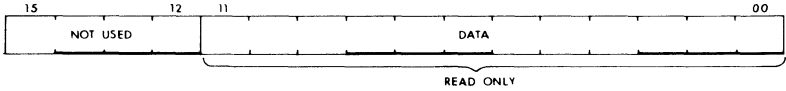
When set, external events initiate A/D conversion.

**03-01 NOT USED**

**00 A/D START**

When set, initiates any A/D conversion.  
Cleared at end of the conversion.

**ANALOG-TO-DIGITAL (A/D) BUFFER REGISTER**



**Bit Name**

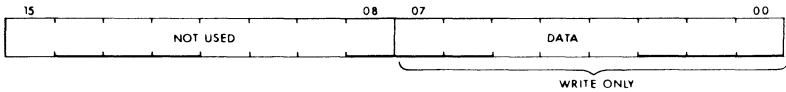
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**15-12 NOT USED**

**11-00 DATA**

These bits contain the digital value of the analog signal after an A/D conversion has been completed.

**DIGITAL-TO-ANALOG (DAC) BUFFER REGISTER**



Note that 1 Least Significant Bit equals 19.4 mV.

**Bit Name**

---

**15-08 NOT USED**

**07-00 DATA**

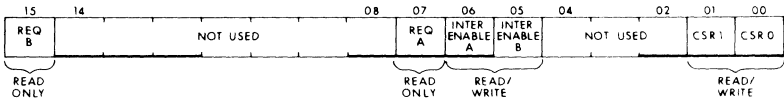
These bits contain the digital value to be converted into an analog signal.

**DR11-C REGISTERS**

The DR11-C general-purpose, digital interface described in Chapter 6 has three registers: the Control and Status register, the Output Buffer

register, and the Input Buffer register. The DR11-C has a floating address which allows the use of more than one DR11-C on a system and avoids address conflicts with other options. Following are the standard register addresses selected for the DR11-C and the applicable register drawings and bit definitions:

**CONTROL AND STATUS REGISTER (CSR) 767770**



**Bit            Name**

**15            REQUEST B**

This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.

When used as an interrupt request, this bit is set by the external device and generates an interrupt provided that INTERRUPT ENABLE B <05> is also set.

When used as a flag, this bit can be read by the program to monitor external device status.

When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 <01>. This permits checking the interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value.

Cleared by INIT.

**14-08        NOT USED**

**07            REQUEST A**

This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program.

When used as an interrupt request, this bit is set by the external device and generates an interrupt provided that INTERRUPT ENBABLE A <06> is also set.

When used as a flag, this bit can be read by the program to monitor external device status.

When the maintenance cable is used, the state of this bit is dependent

on the state of CSR0 <00>. This permits checking the interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value.

Cleared by INIT.

**06 INTERRUPT ENBABLE A**

When set, generates an interrupt if REQUEST A <07> is also set.

Cleared by INIT.

**05 INTERRUPT ENBABLE B**

When set, generates an interrupt if REQUEST B <15> is also set.

Cleared by INIT.

**04-02 NOT USED**

**01 CONTROL AND STATUS 1 (CSR1)**

This bit may be loaded or read under program control from the UNIBUS and used as a user-defined command to the external device. It appears only on Connector No. 1.

When the maintenance cable is used, setting or clearing this bit causes an identical state in REQUEST B <15>. This permits checking the operation of REQUEST <15>, which cannot be loaded by the program.

Cleared by INIT.

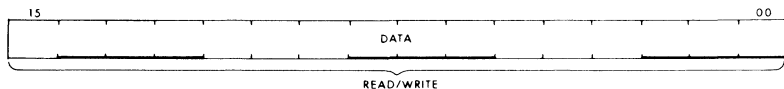
**0 CONTROL AND STATUS 0 (CSR0)**

This bit may be loaded or read under program control from the UNIBUS and used as a user-defined command to the external device. It appears only on Connector No. 2.

When the maintenance cable is used, setting or clearing this bit causes an identical state in REQUEST A <07>. This permits checking the operation of REQUEST <07>, which cannot be loaded by the program.

Cleared by INIT.

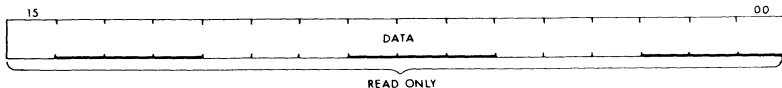
**OUTPUT BUFFER REGISTER (OUTBUF) 767772**



This register is a 16-bit read/write register that may be read or loaded from the UNIBUS under program control.

Cleared by INIT.

**INPUT BUFFER REGISTER (INBUF) 767774**

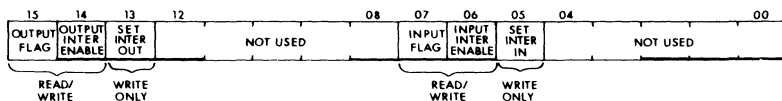


This register is a 16-bit read-only register that receives data from the user's device to be transferred to the UNIBUS.

**DR11-K REGISTERS**

The DR11-K general-purpose, digital interface described in Chapter 6 has the following three registers: the Status register, the Input register, and the Output register. The DR11-K has floating addresses to allow the use of more than one DR11-K on a system and to avoid device address conflicts with other options. Following are the standard register addresses selected for the DR11-K and the applicable register diagrams and bit definitions:

**STATUS REGISTER 167770**



Bit	Name
-----	------

15	<b>OUTPUT FLAG</b>
----	--------------------

Set when an EXTERNAL DATA ACCEPTED signal has been received by the DR11-K from an external device. Cleared under program control.

14	<b>OUTPUT INTERRUPT ENABLE</b>
----	--------------------------------

When set, generates an interrupt when an EXTERNAL DATA ACCEPTED signal has been received by the DR11-K from an external device. Cleared when the interrupt is accepted by the UNIBUS.

13	<b>SET INTERRUPT OUT</b>
----	--------------------------

This bit is used for maintenance only.

## SENSOR I/O DEVICE REGISTERS

When the DR11-K receives this bit, an output interrupt to the UNIBUS is generated.

**12-08 NOT USED**

**07 INPUT FLAG**

Set when an EXTERNAL DATA READY signal has been received by the DR11-K from an external device.

Cleared under program control.

**06 INPUT INTERRUPT ENABLE**

When set, generates an interrupt when an EXTERNAL DATA READY signal has been received by the DR11-K from the external device.

Cleared when the interrupt is accepted by the UNIBUS.

**05 SET INTERRUPT IN**

This bit is used for maintenance only.

When the DR11-K receives this bit, an input interrupt to the UNIBUS is generated.

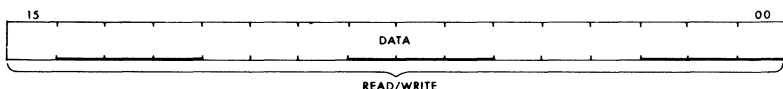
**04-00 NOT USED**

### INPUT REGISTER 167772



This register is a 16-bit read/write register that receives data from an external device to be transferred to the UNIBUS.

### OUTPUT REGISTER 167774

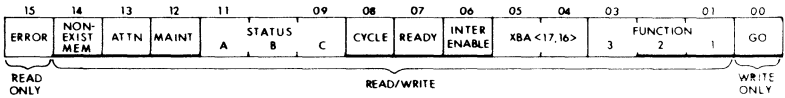


This register is a 16-bit read/write register that may be read or loaded from the UNIBUS under program control.

**DR11-W REGISTERS**

The DR11-W general-purpose, direct memory access (DMA) interface described in Chapter 6 has the following six registers: the Control and Status register, the Error and Information register, the Word Count register, the Bus Address register, the Input Data register, and the Output Data register. The DR11-W has a floating address which allows the use of more than one DR11-W on a system and avoids address conflicts with other options. Following are the standard register addresses selected for the DR11-W and the applicable register drawings and bit definitions:

**CONTROL AND STATUS REGISTER (CSR) 772414**



**Bit Name**

**15 ERROR**

When set, sets READY <07> and prevents further DMA cycles. Generates an interrupt if INTERRUPT ENABLE <06> is also set. Cleared by removing the conditions that caused the bit to set, i.e. ATTENTION <13> and NON-EXISTENT MEMORY <14> in the control and status register, ACLO <11> and MULTI-CYCLE REQUEST <12> in the error and information register. These bits are automatically cleared at the start of the next DMA transfer. ATTENTION <13> and NON-EXISTENT MEMORY <14> may also be cleared by loading with a 0.

**14 NON-EXISTENT MEMORY (NEX)**

When set, indicates that the DR11-W has attempted a transfer to or from a non-existent bus address. Set when the DR11-W asserts MSYN, but does not receive SSYN with 18 μs. When set, sets ERROR <15>, terminates DMA operation, and generates an interrupt if INTERRUPT ENABLE <06> is also set. Cleared by loading with a 0 during INIT or by starting the next DMA transfer.

**13 ATTENTION (ATTN)**

The user's device controls the Attention signal. When asserted, it indicates that a device is on-line.



When set, sets ERROR <15>, generates an interrupt if INTERRUPT ENABLE <06> is also set, and, if a DMA transfer is in progress, stops the transfer at the completion of the current cycle.

Cleared by INIT or at the start of the next DMA transfer.

GO <00> may be set while this bit is set.

**12 MAINTENANCE**

This bit is used for diagnostic testing of the DR11-W.

When set, and CYCLE <08> and GO <00> are also set, the DR11-W starts data transfers that continue until the word count register overflows.

This bit may also be used for software reset.

When set, the DR11-W is in Maintenance mode.

When clear, the DR11-W is initialized.

Cleared by INIT.

**11-09 STATUS A, B, C**

These bits are user-defined and indicate the status of the user's device.

**08 CYCLE**

Set under program control to initiate one NPR operation if GO <00> is also set.

Cleared by INIT and at the start of a bus cycle.

**07 READY**

When set, indicates that the DR11-W has completed the previous operation and is ready to accept a new command.

ERROR <15> must be checked to determine whether or not the transfer was successful. Any error condition must be cleared before a new command can be executed.

Cleared by setting GO <00> or by INIT.

**06 INTERRUPT ENABLE**

When set, generates an interrupt in any of the following conditions: 1) a GO pulse is generated after an error has been detected, 2) the word count register overflows at the end of a data transfer, 3) an error condition signal is detected, i.e. ERROR <15>, NON-EXISTENT MEMORY <14> or ATTENTION <13> in the control and status register, ACLO <11>, MULTI-CYCLE REQUEST <12>, or PARITY ERROR <10> in the error and information register is set during an NPR transfer, or 4) a user device error signal, i.e. ATTENTION <13> is set, is sent to the DR11-W.

Cleared by INIT.

**05-04 EXTENDED BUS ADDRESS (XBA) 17,16**

Loading these bits loads UNIBUS address bits <17, 16>. These bits are incremented when the bus address register overflows. Cleared by INIT.

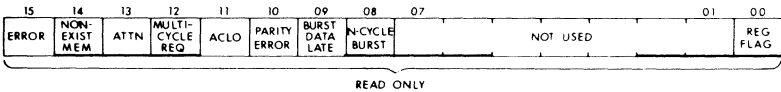
**03-01 FUNCTION 3, 2, 1**

These bits are user-defined and specify the operation to be performed. Cleared by INIT.

**00 GO**

This bit is written under program control and is always read to the UNIBUS as a 0. If this bit is a 1, the error and information register is being read. Setting this bit causes the DR11-W to begin a data transfer.

**ERROR AND INFORMATION REGISTER (EIR) 771414**



Bit	Name

**15 ERROR**

This bit is functionally the same as bit 15 in the control and status register. It is displayed again here for immediate access.

**14 NON-EXISTENT MEMORY**

This bit is functionally the same as bit 14 in the control and status register. It is displayed again here for immediate access.

**13 ATTENTION**

This bit is functionally the same as bit 13 in the control and status register. It is displayed again here for immediate access.

**12 MULTI-CYCLE REQUEST**

Set when a user's device sends a CYCLE REQUEST (A or B) signal to the DR11-W while the DR11-W is still processing the previous transfer. Sets ERROR <15>. Cleared at the start of the next DMA transfer.

**11 ACLO**

When set, indicates that a power failure occurred during a DMA transfer.

Sets Error <15>.

Cleared at the start of the next DMA transfer.

Also cleared by INIT.

**10 PARITY ERROR**

Set whenever the DR11-W detects a memory parity error during a memory read.

Cleared at the start of the next DMA transfer.

**09 BURST DATA LATE**

When set, indicates that the user's device has not supplied or removed data within the established time limit and that the UNIBUS has been relinquished.

The DR11-W is still ready to accept further bus cycle requests.

**08 N-CYCLE BURST**

When set, indicates that the N-Cycle/2-Cycle burst mode switch is set to the N-Cycle position.

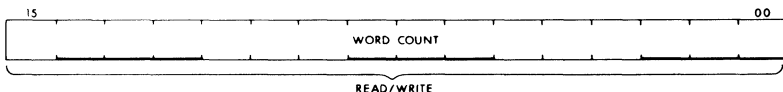
When the DR11-W is set to operate in burst mode, the N-Cycle LED lights to indicated that a burst mode operation is now in progress.

**07-01 NOT USED**

**00 REGISTER FLAG**

If this bit is a 1, it confirms that the error and information register, rather than the control and status register, is being read.

**WORD COUNT REGISTER (WC) 772410**



Before a data transfer, this 16-bit register is loaded with the two's complement of the total number of words to be transferred to or from memory. During subsequent transfers, this register is incremented by one for each word transferred. After transfer of the last word, this register overflows and sets READY <07> in the control and status register, indicating to the user that the data transfer has been completed. If INTERRUPT ENABLE <06> in the control and status register is set, an interrupt occurs after the completion of the last data operation.

**BUS ADDRESS REGISTER (BAR) 762412**



This 16-bit register is loaded with the starting address where data is to be written from or read into memory .

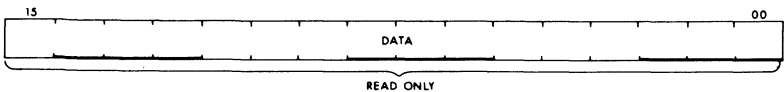
The low-order 16 bits of the bus address are loaded by the bus address register and the high-order 2 bits are loaded by bits <05-04> in the control and status register.

This register is normally incremented by two after an NPR data transfer, so that subsequent transfers are made to consecutive words, i.e the bus address is advanced by two byte-address increments after each transfer.

When this register overflows to all zeros, EXTENDED BUS ADDRESS 17, 16, <04-05> in the control and status register is incremented.

Cleared by INIT.

**INPUT DATA REGISTER (IDR) 762416**



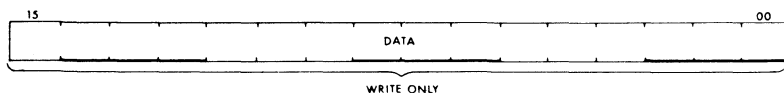
This register is a 16-bit read-only register that receives data from the user's device to be transferred to the UNIBUS.

After completion of a data transfer, the processor can examine the last word transferred by reading this register. This can only be done by writing a 1 into ERROR <15> in the control and status register to set the EIR ENABLE flip-flop in the control logic.

If this register is read when the EIR ENABLE flip-flop is cleared, new data will be sampled from the user's device and clocked into this register. The processor then reads this new data.

Note that EIR functionality is available in DR11-W mode only (it is inhibited in DR11-B mode to provide compatibility).

**OUTPUT DATA REGISTER (ODR) 762416**



This register is a 16-bit write-only register that may be loaded from the UNIBUS under program control or during NPR transfers whenever the DR11-W reads from memory.  
Cleared by INIT.

### IB11 REGISTERS

The IB11 instrument bus interface described in Chapter 6 communicates with devices connected to the IEEE standard instrument bus under program control. The IB11 has two registers: the Instrument Bus Status (IBS) register and the Instrument Bus Data (IBD) register. The IB11 has a floating address which allows the use of more than one IB11 on a system and avoids address conflicts with other options. Following are the standard register addresses selected for the IB11 and the applicable register drawings and bit definitions:

#### INSTRUMENT BUS STATUS REGISTER 160152

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SERV REQ	ERROR 2	ERROR 1	NOT USED		COM DONE	TALKER READY	LISTEN READY	DATA ACCEPT	INTER ENABLE	TALKER ON	LISTEN ON	INTER- FACE BUS CLEAR	REMOTE ON	END OR POLL	TAKE CONTR SYNC
READ/WRITE															

<b>Bit</b>	<b>Name</b>
------------	-------------

#### 15 SERVICE REQUEST (SRQ)

This bit always indicates the status of the instrument bus SRQ line. It may be set and cleared if the ER1 inhibit switch is set to the ON position.

#### 14 ERROR 2 (ER2)

Set when the IB11 tries to send a data or command byte while there is no active listener or command acceptor on the instrument bus. Cleared by clearing TALKER ON <05> or TAKE CONTROL SYNCHRONOUSLY <00>.

#### 13 ERROR 1 (ER1)

Set whenever a conflict occurs between the instrument bus Attention, IFC, or REN lines and their control hardware.

When set, ATN H is cleared and cannot be set. This condition can only be cleared by eliminating the error condition.

This bit may be set when another system controller is connected to the instrument bus. This error may be suppressed by setting the ER1 inhibit switch on the IB11 module to the ON position. If the IB11 is the

only system controller, the ER1 inhibit switch should be set to the OFF position.

**11-12        NOT USED**

**10            COMMAND DONE (CMD)**

When set, indicates to the processor that the IB11 is ready for the next command byte to be transmitted to the DIO lines via the low-byte of the Instrument Bus Data register.

Set by a successful completion of TAKE CONTROL SYNCHRONOUSLY to indicate that the Attention line was asserted and that the next command byte may be transferred over the instrument bus.

Also set when the DAC line is asserted after the command has been accepted by the addressed device on the instrument bus.

Cleared by BINIT L or IFC signals, by writing a command byte into the low-byte of the Instrument Bus Data register, or when TAKE CONTROL SYNCHRONOUSLY <00> is cleared by the program.

**09            TALKER READY (TKR)**

When set, indicates to the processor that the IB11 is ready for the next data byte to be transmitted to the DIO lines via the low-byte of the IBD register.

Set when TALKER ON <05> is set, TAKE CONTROL SYNCHRONOUSLY <00> is clear, and when listeners are ready for data.

Cleared by BINIT L or IFC signals, by writing a command or data byte into the low-byte of the Instrument Bus Data register, when TALKER ON <05> is cleared by the program, or when TAKE CONTROL SYNCHRONOUSLY <00> is set by the program.

**08            LISTENER READY (LNR)**

When set, indicates that the IB11 has a data or command byte that is ready to be read from the low-byte of the Instrument Bus Data register. Set when LISTENER ON <04> is set and the DAV line is asserted.

Cleared by reading the low-byte from the Instrument Bus Data register if ACCEPT DATA <07> is clear or by clearing the low-byte of the Instrument Bus Data register if ACCEPT DATA <07> is set.

Also cleared when LISTENER ON <04> is cleared by the program.

Also cleared by BINIT L and IFC signals.

**07            ACCEPT DATA (ACC)**

Set and cleared under program control.

When clear, reading a data byte from the Data Input/Output (DIO)

lines will automatically assert the DAC line and clear LISTENER READY <08>.

When set, the program must clear the low-byte of the Instrument Bus Data register in order to clear LISTENER READY <08> and assert the DAC line.

Also cleared by BINIT L or IFC signals when LISTENER ON <04>, TALKER ON <05>, and TAKE CONTROL SYNCHRONOUSLY <00> are clear.

May be set to assert the NRFD line.

**06 INTERRUPT ENABLE (IE)**

Set and cleared under program control to enable or disable IB11 interrupts.

When set, enables interrupts.

When clear, disables interrupts.

Also cleared by BINIT L signal.

**05 TALKER ON (TON)**

Set or cleared under program control to enable or disable the IB11 talker function.

Also cleared by BINIT L or IFC signals.

**04 LISTENER ON (LON)**

Set or cleared under program control to enable or disable the IB11 listener function.

When set and the DAV line is asserted, LISTENER READY <08> is set.

When clear, the IB11 ignores the DAV line.

Also cleared by BINIT L or IFC signals.

**03 INTERFACE BUS CLEAR (IBC)**

When set, the leading edge of the IBC signal produces an IFC signal for approximately 125  $\mu$ s.

At the end of the IFC signal (125  $\mu$ s), TAKE CONTROL SYNCHRONOUSLY <00> is automatically set and this bit is automatically cleared.

Also cleared by BINIT L signal.

**02 REMOTE ON (REM)**

Set or cleared under program control to assert or unassert the REMOTE ENABLE (REN) line.

Also cleared by BINIT L or IFC signals.

**01 END OR POLL (EOP)**

Set or cleared under program control to assert or unassert the End Or Identify (EOI) line.

Also cleared by BINIT L or IFC signals.

**00 TAKE CONTROL SYNCHRONOUSLY (TCS)**

Set or cleared under program control to enable or disable the IB11 controller-in-charge function by taking control synchronously or by negating the Attention (ATN) control line in the instrument bus.

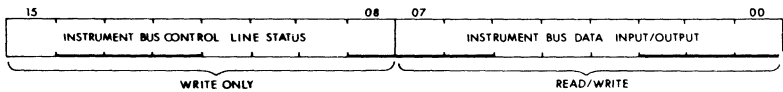
When set, causes the Not Ready For Data (NRFD) line to be asserted for at least 500 ns before Data Valid (DAV) is checked.

If DAV is not asserted, the instrument bus Attention line is asserted.

If NRFD is not asserted, then whenever the Attention line is asserted, COMMAND DONE <10> will be set 500 ns after the Attention line is asserted.

Also cleared by the Bus Initialize Signal (BINIT L) and the Interface Clear (IFC) signal.

**INSTRUMENT BUS DATA REGISTER 160150**



**15-08 INSTRUMENT BUS CONTROL LINE STATUS**

These eight bits correspond to the eight instrument bus control signal lines. The program can monitor the status of all eight control signal lines by reading this byte. Note that DAC <08> and RFD <10> are inverted with respect to the actual instrument bus signal lines.

**07-00 INSTRUMENT BUS DATA INPUT/OUTPUT**

These eight bits correspond to the eight instrument bus data lines. The program can read or write via this register byte to receive or transmit command or data bytes over the instrument bus.

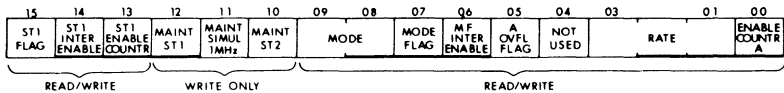
**KW11-K REGISTERS**

The KW11-K dual-programmable realtime clock described in Chapter 6 has the following six registers: the A Status register, the A Pre-set/Buffer register, the A Counter register, the B Status register, the B Buffer register, and the B Counter register. The KW11-K has a floating address which allows the use of more than one KW11-K on a system



and avoids address conflicts with other options. Following are the standard register addresses selected for the KW11-K and the applicable register drawings and bit definitions:

**A STATUS REGISTER 770404**



**Bit                      Name**

**15                      ST1 FLAG**

When set, indicates that a ST1 event or a maintenance ST1 event has occurred.

**14                      ST1 INTERRUPT ENABLE**

When set, generates an interrupt if an ST1 event has occurred.

**13                      ST1 ENABLE COUNTER**

When set, sets ENABLE COUNTER A <00> when an ST1 event has occurred.

**12                      MAINTENANCE ST1**

This bit is used for maintenance only.

When set, generates an ST1 event.

**11                      MAINTENANCE SIMULATION 1 MHz**

This bit is used for maintenance only.

When set, generates a 1 MHz clock pulse in clock A.

**10                      MAINTENANCE ST2**

This bit is used for maintenance only.

When set, generates an ST2 event.

**09-08                  MODE**

These bits are loaded to select the mode of operation of clock A. Following are the modes of operation which may be selected:

## SENSOR I/O DEVICE REGISTERS

Bit 09	Bit 08	Mode of Operation
0	0	<p><b>Single Interval Mode</b></p> <p>The counter in clock A counts from preset value to overflow, sets MODE FLAG &lt;07&gt; and A OVERFLOW FLAG &lt;05&gt; (if jumper W2 is installed) in the A Status register, transfers the A Preset/Buffer register contents to the A Counter register and stops. Overflow generates an A Event Output signal to an external device.</p>
0	1	<p><b>Repeated Interval Mode</b></p> <p>The counter in clock A counts from preset value to overflow, sets MODE FLAG &lt;07&gt; and A OVERFLOW FLAG &lt;05&gt; (if jumper W2 is installed) in the A Status register, transfers the A Preset/Buffer register contents to the A Counter register and begins again. Overflow generates an A Event Output signal to an external device.</p>
1	0	<p><b>External Event Time Mode</b></p> <p>The counter in clock A is free-running at the selected rate and a pulse from ST2 transfers the contents of the A Counter register to the A Preset/Buffer register, sets MODE FLAG &lt;07&gt; in the A Status register, and continues counting.</p>
1	1	<p><b>External Event Time Mode From Zero Base</b></p> <p>The counter in clock A is free-running at the selected rate and a pulse from ST2 transfers the contents of the A Counter register to the A Preset/Buffer register, sets MODE FLAG &lt;07&gt;, clears the A Counter register, and continues counting from zero.</p>

## SENSOR I/O DEVICE REGISTERS

### 07            **MODE FLAG**

Sets on overflow or when a Counter-to-Buffer Transfer operation occurs.

### 06            **MODE FLAG INTERRUPT ENABLE**

When set, generates an interrupt if MODE FLAG <07> is set.

### 05            **A OVERFLOW FLAG**

Sets on overflow from A Counter register (if jumper W2 is installed).

### 04            **NOT USED**

### 03-01        **RATE**

These bits are loaded to select the rate at which clock A operates. Following are the rates which may be selected:

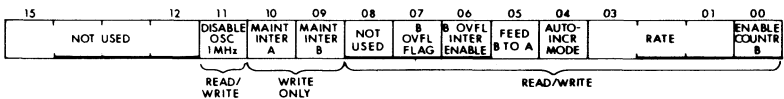
Bit 03	Bit 02	Bit 01	Clock A
0	0	0	No rate or clock B overflow
0	0	1	1 MHz
0	1	0	100 KHz
0	1	1	10 KHz
1	0	0	1 KHz
1	0	1	100 Hz
1	1	0	STP1
1	1	1	Line frequency

### 00            **ENABLE COUNTER A**

When set, enables clock A to count at the selected rate.

Set either by program-control or by ST1 INTERRUPT ENABLE <14>.

## **B STATUS REGISTER 770432**



### 15-12        **NOT USED**

### 11            **DISABLE OSCILLATOR 1 MHz**

When set, disables the 1 MHz oscillator in clock A that is used to generate the other crystal-controlled frequencies for clock A.

**10 MAINTENANCE INTERRUPT A**

This bit is used for maintenance only.  
When set, generates a clock A interrupt.

**09 MAINTENANCE INTERRUPT B**

This bit is used for maintenance only.  
When set, generates a clock B interrupt.

**08 NOT USED**

**07 B OVERFLOW FLAG**

Sets on overflow from clock B.

**06 B OVERFLOW INTERRUPT ENABLE**

When set, generates an interrupt on overflow from clock B.

**05 FEED B TO A**

When set and clock A is selected for rate 0, the overflow from clock B is used as the clocking frequency for clock A.

**04 AUTO-INCREMENT MODE**

When set, the A Preset/Buffer register is decremented by two's complement on overflow from clock A.

When set and an ST2 occurs, the internal KW11-K clock timing is synchronized to it.

**03-01 RATE**

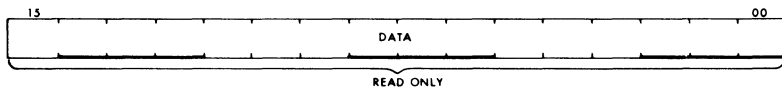
These bits are loaded to select the rate at which clock B operates. Following are the rates which may be selected:

Bit 03	Bit 02	Bit 01	Clock B
0	0	0	No rate
0	0	1	1 MHz
0	1	0	100 KHz
0	1	1	10 KHz
1	0	0	1 KHz
1	0	1	100 Hz
1	1	0	STP3
1	1	1	Line frequency

**00            ENABLE COUNTER B**

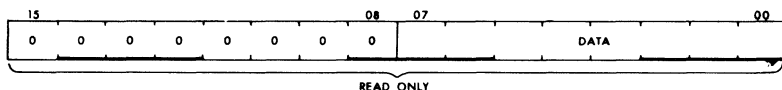
When set, enables clock B to count at the selected rate.

**A COUNTER REGISTER 770430**



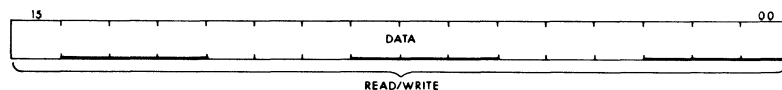
This register is a 16-bit (word-oriented) counter that keeps track of the number of clock pulses that have elapsed since the clock was initiated. It is a read-only register and may be read while clock A is in operation.

**B COUNTER REGISTER 770436**



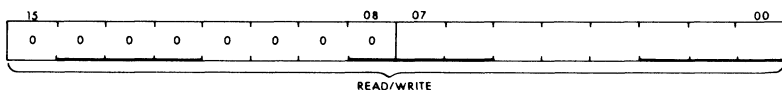
This register is an 8-bit (low-byte) counter that keeps track of the number of clock pulses that have elapsed since the clock was initiated. It is a read-only register that may be read only while clock B is not in operation.

**A PRESET/BUFFER REGISTER 770406**



This register is a 16-bit (word-oriented) register that stores the timing data for the A clock. It is a read/write register that may be written into or read while clock A is in operation.

**B BUFFER REGISTER 770434**



This register is an 8-bit (low-byte) register that stores the timing data for the B clock. It is a read/write register that may be written into or read only while clock B is not in operation.

**LPA11-K REGISTERS**

The LPA11-K intelligent, direct memory access (DMA) subsystem described in Chapter 6 has the following three registers: the Control In/Maintenance register, the Control Out/Status Out register, and the Command Address register. The LPA11-K has a floating address which allows the use of more than one LPA11-K on a system and avoids address conflicts with other options. Following are the standard register addresses selected for the LPA11-K and the applicable register drawings and bit definitions:

**CONTROL IN/MAINTENANCE REGISTER 170460**

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
RUN	RESET	CRAM WRITE	NOT USED	ENABLE ARBIT	ROM OUTPUT	NOT USED	NOT USED	READY IN	IN INTER ENABLE	NOT USED	NOT USED	BUS ADDRESS 17, 16	NOT USED	NOT USED	GO

**Bit            Name**

---

**15            RUN**

When set, starts the master microprocessor.  
When cleared, stops the master microprocessor.

**14            RESET**

When set, initializes the LPA11-K subsystem including all I/O devices.

**13            CRAM WRITE**

This bit is used in loading the microcode.

**12            NOT USED**

**11            ENABLE ARBITRATION**

When set, enables the LPA11-K intermicroprocessor buffer (IPB) to arbitrate nonprocessor (NPR) requests and bus requests (BR) between the slave microprocessor and the devices on the I/O bus.  
When clear, the normal arbitration logic is inhibited.  
Cleared by INIT.

**10            ROM OUTPUT**

This bit is used in loading the microcode.

**09-08        NOT USED**

## SENSOR I/O DEVICE REGISTERS

### 07            **READY IN**

When set, the LPA11-K is ready to accept a new command from the host processor.

Cleared when RDA processing is initiated by the LPA11-K.

### 06            **IN INTERRUPT ENABLE**

When set, allows interrupts to be generated when READY IN <07> is set.

### 05-04        **NOT USED**

### 03            **BUS ADDRESS 17**

This bit contains extended memory address bit <17> of the command address. It is used in conjunction with BUS ADDRESS 16 <02> and the bus address register (which contains the low-order 16 bits of the bus address) to specify the address of the next command for the LPA11-K in main memory.

### 02            **BUS ADDRESS 16**

This bit contains extended memory address bit <16> of the command address. It is used in conjunction with BUS ADDRESS 17 <03> and the bus address register (which contains the low-order 16 bits of the bus address) to specify the address of the next command for the LPA11-K in main memory.

### 01            **NOT USED**

### 00            **GO**

When set, indicates that a new command address is now available for processing by the LPA11-K.

Cleared by the LPA11-K during the user request initiation.

## CONTROL OUT/STATUS OUT REGISTER 170462

15	14	13	12	08	07	06	05	03	02	00
STATUS/ ERROR INDIC	ERROR STATUS 0 AND 1		ERROR CODE 0 - 4		READY OUT	OUT INTER ENABLE	NOT USED		USER INDEX	

## SENSOR I/O DEVICE REGISTERS

**Bit**            **Name**

---

**15**            **STATUS/ERROR INDICATOR**

When set, indicates that an error condition has been detected by the LPA11-K.

When clear, indicates a status condition.

**14-13**        **ERROR STATUS 0 and 1**

These bits indicate the conditions which caused the error or status condition specified by STATUS/ERROR INDICATOR <15>.

**12-08**        **ERROR CODE 0-4**

These bits indicate the error or status condition of the LPA11-K.

**07**            **READY OUT**

When set, indicates that the LPA11-K has status information to report to the host processor.

Cleared by the host processor to acknowledge the reception of the status information.

**06**            **OUT INTERRUPT ENABLE**

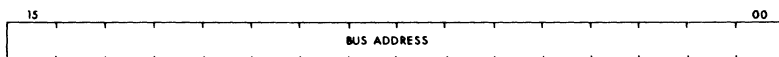
When set, allows an interrupt to be generated when READY OUT <07> is set.

**05-03**        **NOT USED**

**02-00**        **USER INDEX**

These bits contain a 3-bit octal code assigned by the LPA11-K to associate the status condition to one of the eight user requests.

### COMMAND ADDRESS REGISTER 170464



This register contains the low-order 16 bits of the bus address and is used in conjunction with BUS ADDRESS 17 <03> and BUS ADDRESS 16 <02> to specify the address of the next command for the LPA11-K in main memory.



**APPENDIX A**

**STANDARD AND COMPRESSED HOLLERITH CODE**

CHARACTER	ROWS PUNCHED	STANDARD CODE (OCTAL)	COMPRESSED CODE (OCTAL)
Space	None	0000	000
0	10	1000	040
1	1	0400	001
2	2	0200	002
3	3	0100	003
4	4	0040	004
5	5	0020	005
6	6	0010	006
7	7	0004	007
8	8	0002	010
9	9	0001	020
&	12	4000	200
—	11	2000	100
A	12, 1	4400	201
B	12, 2	4200	202
C	12, 3	4100	203
D	12, 4	4040	204
E	12, 5	4020	205
F	12, 6	4010	206
G	12, 7	4004	207
H	12, 8	4002	210
I	12, 9	4001	220
:	12, 11	6000	300
{	12, 10	5000	240
}	11, 10	3000	140
J	11, 1	2400	101
K	11, 2	2200	102
L	11, 3	2100	103
M	11, 4	2040	104
N	11, 5	2020	105
O	11, 6	2010	106
P	11, 7	2004	107
Q	11, 8	2002	110
R	11, 9	2001	120
/	10, 1	1400	051
S	10, 2	1200	042
T	10, 3	1100	043
U	10, 4	1040	044
V	10, 5	1020	045
W	10, 6	1010	046
X	10, 7	1004	047
Y	10, 8	1002	050

APPENDIX A

STANDARD AND COMPRESSED HOLLERITH CODE (Cont.)

CHARACTER	ROWS PUNCHED	STANDARD CODE (OCTAL)	COMPRESSED CODE (OCTAL)
Z	10, 9	1001	060
`	8, 1	0402	011
:	8, 2	0202	012
#	8, 3	0102	013
@	8, 4	0042	014
'	8, 5	0022	015
=	8, 6	0012	016
"	8, 7	0006	017
a	12, 10, 1	5400	241
b	12, 10, 2	5200	242
c	12, 10, 3	5100	243
d	12, 10, 4	5040	244
e	12, 10, 5	5020	245
f	12, 10, 6	5010	246
g	12, 10, 7	5004	247
h	12, 10, 8	5002	250
i	12, 10, 9	5001	260
j	12, 11, 1	6400	301
k	12, 11, 2	6200	302
l	12, 11, 3	6100	303
m	12, 11, 4	6040	304
n	12, 11, 5	6020	305
o	12, 11, 6	6010	306
p	12, 11, 7	6004	307
q	12, 11, 8	6002	310
r	12, 11, 9	6001	320
[	12, 8, 2	4202	212
.	12, 8, 3	4102	213
<	12, 8, 4	4042	214
(	12, 8, 5	4022	215
+	12, 8, 6	4012	216
! or †	12, 8, 7	4006	217
~	11, 10, 1	3400	141
s	11, 10, 2	3200	142
t	11, 10, 3	3100	143
u	11, 10, 4	3040	144
v	11, 10, 5	3020	145
w	11, 10, 6	3010	146
x	11, 10, 7	3004	147
y	11, 10, 8	3002	150
z	11, 10, 9	3001	160

## APPENDIX A

## STANDARD AND COMPRESSED HOLLERITH CODE (Cont.)

CHARACTER	ROWS PUNCHED	STANDARD CODE (OCTAL)	COMPRESSED CODE (OCTAL)
	11, 8, 2	2202	112
\$	11, 8, 3	2102	113
*	11, 8, 4	2042	114
)	11, 8, 5	2022	115
:	11, 8, 6	2012	116
Λ or ∩	11, 8, 7	2006	117
\	10, 8, 2	1202	051
.	10, 8, 3	1102	052
%	10, 8, 4	1042	054
—	10, 8, 5	1022	055
>	10, 8, 6	1012	056
?	10, 8, 7	1006	057



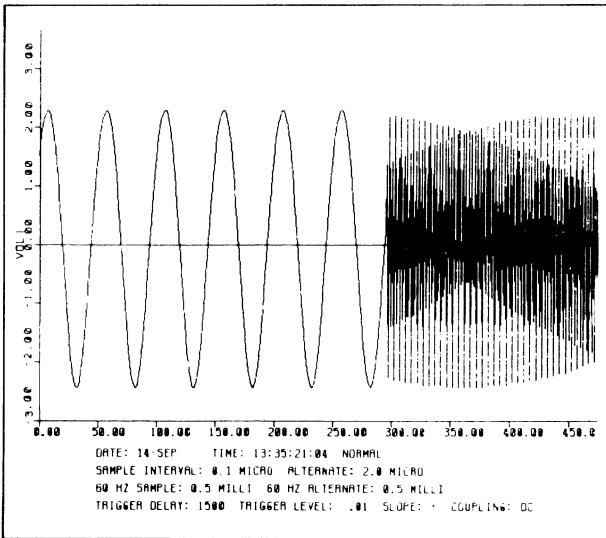
# EXAMPLES OF LXY11/LXY211 PRINT COPY AND GRAPHICS

```

=>?@ABCDEFGHIJKLMNQPQRSTUVWXYZ[\

^ `abcdefghijklmnopqrstuvwxyz{!}
!+,-./0123456789:;<=>?@ABCDEFGHI
{!}^ `abcdefghijklmnopqrstuvwxyz
>?@ABCDEFGHIJKLMNQPQRSTUVWXYZ[\
^ `abcdefghijklmnopqrstuvwxyz{!}
:~?@ABCDEFGHIJKLMNQPQRSTUVWXYZ[\
!z{!}^ `abcdefghijklmnopqrstuvw

```





# APPENDIX C

## 7-BIT ASCII CODE

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	@	140	\
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	\$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	-	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	
035	GS	075	=	135	]	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	_	177	DEL





**APPENDIX D**

**UNIBUS I/O PAGE DEVICE  
ADDRESSES AND VECTOR ASSIGNMENTS**

<b>Device</b>	<b>Address</b>	<b>Size in Words</b>	<b>Number of Devices</b>	
AA11	776750	8	1	(first unit)
AA11	776400	8	4	(extra units)
AD01	776770	4	1	
ADF11	770460	8	1	
AFC11	772570	4	1	
AR11	770400	8	1	
BM792-YA	773000	32	1	
BM792-YB	773100	32	1	
BM792-YC	773200	32	1	
BM792-YH	773300	32	1	
BM873-YA	773000	128	1	
BM873-YB	773000	256	1	
BM873-YC	773000	256	1	
CD11	777160	4	1	
CM11	777160	4	1	
CR11	777160	4	1	
Customer	764000	1024	1	
DC11	774000	4	32	
DC14-D	777360	8	1	
Diagnostics	760000	4	1	
DL11-A	777560	4	1	(console)
DL11-A	776500	4	16	
DL11-B	777560	4	1	(console)
DL11-B	776500	4	16	
DL11-C	775610	4	31	
DL11-D	775610	4	31	
DL11-E	775610	4	31	
DL11-W	777546	1	1	(line clock, first unit only)
DL11-W	777560	4	1	(console)
DL11-W	776500	4	16	
DM11	775000	4	16	
DM11-BB	770500	4	16	(modem control for DM11)
DN11-AA	775200	4	16	

APPENDIX D

Device	Address	Size in Words	Number of Devices	
DN11-DA	775200	1	64	
DP11	774400	4	-32	(assigned backwards)
DR11-A/C	767600	4	-16	(assigned backwards)
DR11-B(1)	772410	4	1	
DR11-B(2)	772430	4	1	
DS11	775400	67	1	
DT11	777420	1	8	
DV11	775000	16	4	
DX11	776200	16	2	
Floating CSRs	760010	1020	1	
FP11	772160	8	1	
GT40	772000	4	4	
ICR/ICS11	771000	256	1	
IP11/IP300	771000	128	2	
KE11	777300	8	2	
KG11	770700	4	8	
KL11	776500	4	16	
KL11	777560	4	1	(console)
KT11	772200	64	1	
KT11-SR3	772516	1	1	
KU116-AA	777540	1	1	
KW11-L	777546	1	1	
KW11-P	772540	4	1	
KW11-W	772400	4	1	
LP11	777514	2	1	(LP0)
LP11	764004	2	1	(LP1)
LP11	764014	2	1	(LP2)
LP11	764024	2	1	(LP3)
LP11	764034	2	1	(LP4)
LP11	764044	2	1	(LP5)
LP11	764054	2	1	(LP6)
LP11	764064	2	1	(LP7)
LP20	775400	32	2	
LPA11-K	770460	8	1	
LPS11	770400	16	1	
LS11	777514	2	1	
LV11	777514	2	1	
M792	773000	32	8	

## APPENDIX D

<b>Device</b>	<b>Address</b>	<b>Size in Words</b>	<b>Number of Devices</b>	
M9301-XX	765000	256	1	
M9301-XX	773000	256	1	
MM11-LP	772100	1	16	
MR11-DB	773100	64	1	
MS11-K	772100	1	16	
MS11-LP	772100	1	16	
NCV11	772760	8	1	
OST	772500	6	1	
PA611_readers	772600	32	1	(2 per PA611)
PA611_punches	772700	32	1	(2 per PA611)
PC11	777550	4	1	
PDP-11/04	777570	68	1	
PDP-11/05	777570	68	1	
PDP-11/10	777570	68	1	
PDP-11/15	777570	68	1	
PDP-11/20	777570	68	1	
PDP-11/24	777570	68	1	
PDP-11/34A	777570	68	1	
PDP-11/35	777570	68	1	
PDP-11/40	777570	68	1	
PDP-11/44	777570	68	1	
PDP-11/45	777570	68	1	
PDP-11/55	777570	68	1	
PDP-11/60	777570	68	1	
PDP-11/70	777570	68	1	
PR11	777550	4	1	
RC11	777440	8	1	
Reserved	770100	32	1	
Reserved	770440	8	1	
Reserved	772150	4	1	
Reserved	772420	4	1	
Reserved	772514	1	1	
Reserved	772550	8	1	
Reserved	775606	1	1	
Reserved	777000	56	1	
Reserved	777200	32	1	
Reserved	777510	2	1	
Reserved	777520	4	1	
Reserved	777540	3	1	
RF11	777460	8	1	

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Device	Address	Size in Words	Number of Devices	
RH70/11_alt	776300	32	1	(Alternate RS/RP/RM/TJ)
RK611	777440	16	1	
RK11	777400	8	1	
RL11	774400	4	1	
RM03/04/05	776700	22	1	(RH70/RH11)
RP04/05/06	776700	22	1	(RH70/RH11)
RP11	776700	16	1	(RH70/RH11)
RS04	772040	16	1	(RH70/RH11)
RX11/RX211	777170	4	1	
TA11/DIP11-A	777500	4	1	
TC11	777340	8	1	
Testers	770000	32	1	
TM11/TMB11	772520	8	1	
TR79	764000	4	1	
TS11	772520	2	4	
TU16/45/77	772440	16	1	(RH70/RH11)
TU58	776500	4	4	
UDC-Units	771000	1	256	
UDC11	771774	2	1	
UET	772140	4	1	
Unibus-Map	770200	64	1	
VSV11	772000	4	4	
VT48	772000	16	1	
VTV01	772600	112	2	
XY11	777530	4	1	

**PDP-11 INTERRUPT AND TRAP VECTORS**

000	PDP-11 Reserved
004	PDP-11 CPU Errors (Illegal instructions, Bus Errors, Stack Limit, Illegal Internal Address, Microbreak)
010	PDP-11 Reserved Instructions
014	PDP-11 Breakpoint/Trace traps
020	PDP-11 IOT Trap
024	PDP-11 Power Fail
030	PDP-11 EMT Trap
034	PDP-11 TRAP Trap
040	Reserved for System Software

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044	Reserved for System Software
050	Reserved for System Software
054	Reserved for System Software
060	DL11(1), KL11(1)
064	DL11(1), KL11(1)
070	PC11, paper tape reader
074	PC11, paper tape punch
100	KW11-L, line clock
104	KW11-P, programmable clock
110	Reserved for System Software
114	CPU
120	XY11, Plotter
124	DR11-B, DMA interface
130	AD01, A/D subsystem
134	AFC11, analog subsystem
140	AA11, display
144	AA11, RSTS/E (crash-dump)
150	alternate RS/RP/RM/TJ
154	UNUSED - Reserved for Digital
160	RL11, disk
164	UNUSED - Reserved for Digital
170	LP/LS/LV11 (#1), USER RESERVED
174	LP/LS/LV11 (#2), USER RESERVED
200	LP/LS/LV11 (#0), LP20 (1), lineprinter
204	RF11, RS03/04 (RH11/RH70), MASSBUS fixed head disk
210	LP20(2), RC11, RK611/RK711
214	TC11, DECTape
220	RK11, disk
224	TM11, TS11, TU16/45, TE16, TU77, MASSBUS Magnetic tape
230	CD11, CM11, CR11
234	ICS/ICR11, IP11/IP300, UDC11
240	PDP-11-PIRQ
244	Floating Point exception
250	Memory Management error
254	RM02/03/50 (RH11/RH70), RP04/5/6 (RH11/RH70), RP11
260	DiP11, TA11
264	RX11, floppy disk
270	LP/LS/LV11 (#3), USER RESERVED
274	LP/LS/LV11 (#4), USER RESERVED
300	Floating Vectors

**FLOATING VECTORS**

There is a floating vector convention used for communications and other devices that interface with the PDP-11. These vector addresses are assigned in order starting at 300 and proceeding upwards to 777. The following Table shows the assigned sequence. It can be seen that the first vector address, 300, is assigned to the first DC11 in the system. If another DC11 is used, it would then be assigned vector address 310, etc. When the vector addresses have been assigned for all the DC11s (up to a maximum of 32), addresses are then assigned consecutively to each unit of the next highest-ranked device (KL11 or DP11 or DM11, etc.), then to the other devices in accordance with the priority ranking.

**Priority Ranking for Floating Vectors**

(starting at 300 and proceeding upwards)

<b>Rank</b>	<b>Option</b>	<b>Decimal Size (words)</b>	<b>Octal Modulus (address)</b>
1	DC11	4	10
1	TU58	4	10 (See Note 1)
2	KL11(extra)	4	10
2	DL11-A(extra)	4	10
2	DL11-B(extra)	4	10
3	DP11	4	10
4	DM11-A	4	10
5	DN11	2	4
6	DM11-BB	2	4
7	DH11 modem control	2	4
8	DR11-A	4	10
9	DR11-C	4	10
10	PA611(reader+punch)	8	10
11	LPD11	4	10
12	DT11	4	10
13	DX11	4	10
14	DL11-C	4	10
14	DL11-D	4	10
14	DL11-E	4	10
15	DJ11	4	10

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Rank	Option	Decimal Size (words)	Octal Modulus (address)
16	DH11	4	10
17	GT40	8	10
17	VSV11	8	10
18	LPS11	12	10
19	DQ11	4	10
20	KW11-W	4	10
21	DU11	4	10
22	DUP11	4	10
23	DV11+modem control	6	10
24	LK11-A	4	10
25	DWUN	4	10
26	DMC11	4	10
26	DMR11	4	10 (DMC before DMR)
27	DZ11	4	10
28	KMC11	4	10
29	LPP11	4	10
30	VMV21	4	10
31	VMV31	4	10
32	VTV01	4	10
33	DWR70	4	10
34	RL11/RLV11	2	4 (after the first)
35	RX02	2	4
36	TS11	2	4 (after the first)
37	LPA11-K	4	10
38	IP11/IP300	2	4
39	KW11-C	4	10
40	RX11	2	4 (after the first)
41	DR11-W	2	4
42	DR11-B	2	4 (after the first)

1 There is no standard configuration for systems with both DC11 and TU58.

**FLOATING CSR ADDRESS DEVICES**

There is a floating address convention used for communications and other devices interfacing with the PDP-11. These addresses are assigned in order starting at 760 010 and proceeding upwards to 763 776. Floating addresses are assigned in the following sequence:

Rank	Option	Decimal Size (words)	Octal Modulus (address)
1	DJ11	4	10
2	DH11	8	20
3	DQ11	4	10
4	DU11	4	10
5	DUP11	4	10
6	LK11A	4	10
7	DMC11/DMR11	4	10 (DMC before DMR)
8	DZ11 <sup>1</sup> and DZV11	4	10
9	KMC11	4	10
10	LPP11	4	10
11	VMV21	4	10
12	VMV31	8	20
13	DWR70	4	10
14	RL11 and RLV11	4	10 (extra only)
15	LPA11-K	8	20 (extra only)
16	KW11-C	4	10
17	Reserved	4	10
18	RX11	4	10 (extra only)
19	DR11-W	4	10
20	DR11-B	4	10 (after second)

1 DZ11E and DZ11F are dual DZ11s and are treated by the algorithm as two DZ11s.

**DEVICE ADDRESSES**

776 000	} Diagnostics
760 006	
760 010	(Start of floating addresses)
763 776	(Top of floating addresses)



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764 000	TR79	
764 004	LP11(#0-7)	} Customer
764 066		
765 000		
765 776		
	M9301	
767 600	DR11-A/C	}
767776		
770 000	Testers	}
770 076		
770 100	Reserved	}
770 176		
770 200	UNIBUS Map	}
770 376		
770 400	AR11	} LPS11
770 416		
770 436		
770 440	Reserved	}
770 456		
770 460	ADF11/LPA11-K	}
770 476		
770 500	DM11-BB	#1
770 676		#16

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770 700 } 770 776 }	KG11	#1 #8	
771 000 } 771 776 }	UDC Functional I/O Units		ICR/ICS11 IP11/IP300
771 774 } 771 776 }	UDC11		ICR/ICS11 IP11/IP300
772 000 } 772 036 }	GT40 (#1-#4) VSV11 (#1-#4) VT48		
772 040 } 772 076 }	RS04		
772 100 } 772 136 }	UNIBUS Memory Parity		MM11-LP #1 MS11-LP #16
772 140 } 772 146 }	UNIBUS Tester		
772 150 } 772 156 }	Reserved		
772 160 } 772 176 }	FP11 Registers		
772 200 } 772 216 }	Supervisor Instruction Descriptor PDR, reg 0-7		
772 220 } 772 236 }	Supervisor Data Descriptor PDR, reg 0-7		

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772 240 )	Supervisor Instruction PDR, reg 0-7
772 256 )	
772 260 )	Supervisor Data PAR, reg 0-7
772 276 )	
772 300 )	Kernel Instruction PDR, reg 0-7
772 316 )	
772 320 )	Kernel Data PDR, reg 0-7
772 336 )	
772 340 )	Kernel Instruction PAR, reg 0-7
772 356 )	
772 360 )	Kernel Data PAR, reg 0-7
772 376 )	
772 400 )	KW11-W
772 406 )	
772 410 )	DR11-B (#1)
772 416 )	
772 420 )	Reserved
772 426 )	
772 430 )	DR11-B (#2)
772 436 )	
772 440 )	TU16/45/77
772 476 )	

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772 500	}	OST	
772 512			
772 514		Reserved	
772 516		Memory Mgt. reg (MMR3)	
772 520	}	TM11/TMB11/TS11	
772 536			
772 540	}	KW11-P	
772 546			
772 550	}	Reserved	
772 566			
772 570	}	AFC11	
772 576			
772 600	}	PA611 Typeset Readers	
772 676			
772 700	}	PA611 Typeset Punches	} VTV01
772 776			
772 760	}	NCV11	
772 776			
773 476			

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773 000 )	BM792-YA	}	BM873-YA	}	BM873-YB
773 076 )					
773 100 )	MR11-DB	}		}	BM873-YC
773 276 )					
773 376 )					
773 776 )					
774 000 )	DC11,	}	#1	}	
774 376 )			#32		
774 400 )	RL11	}		}	#1
774 406 )			DP11,		
774 776 )			#32		
775 000 )	DM11,	}	#1	}	DV11, #1-#4
775 176 )			#16		
775 200 )	DN11-AA/DN11-DA	}		}	#1
775 376 )			#16		
775 400 )	LP20	}	DS11	}	
775 576 )					
775 604 )					
775 606 )	Reserved				
775 610 )	DL11-C, -D, -E	}	#1	}	
776 176 )			#31		
776 200 )	DX11	}		}	
776 276 )					

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776 300 } 776 376 }	alternate RH70/RH11	
776 400 } 776 476 }	AA11, #2 #5	
776 500 } 776 676 }	TU58 DL11-A, -B, -W #16	KL11, #1
776 700 } 776 736 } 776 752 }	RP11 }	RM03/04/05, RP04/05/06
776 750 } 776 766 }	AA11, #1	
776 770 } 776 776 }	AD01	
777 000 } 777 156 }	Reserved	
777 160 } 777 166 }	CM11, CD11 CR11	
777 170 } 777 176 }	RX11/RX211	
777 200 } 777 276 }	Reserved	

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777 300 )	KE11, #2		
777 336 )			
777 340 )	TC11		
777 356 )			
777 360 )	DC14-D		
777 376 )			
777 400 )	RK11		
777 416 )			
777 420 )	DT11		
777 436 )			
777 440 )	RC11 )	RK611	
777 456 )			
777 460 )			
777 476 )			
777 500 )	TA11/DIP11-A		
777 506 )			
777 510 )	Reserved		
777 512 )			
777 514 )	LP11/LS11/LV11		
777 516 )			
777 520 )	Reserved		
777 526 )			

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777 530	} XY11
777 536	
770 540	} KV116-AA
777 544	
777 546	DL11-W/KW11-L, line clock
777 550	} PC11/PR11
777 556	
777 560	} DL11-A/DL11-B Console Terminal
777 566	
777 570	Console Switch & Display Register
777 572	(MMR0)
777 574	Memory Mgt. reg (MMR1)
777 576	(MMR2)
777 600	} User Instruction PDR, reg 0-7
777 616	
777 620	} User Data PDR, reg 0-7
777 636	
777 640	} User Instruction PAR, reg 0-7
777 656	
777 660	} User Data PAR, reg 0-7
777 676	



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777 700		R0
777 701		R1
777 702	General registers, Set 0	R2
777 703		R3
777 704		R4
777 705		R5
777 706	Kernel	R6 (SP)
777 707		R7 (PC)
777 710		R0
777 711		R1
777 712	General registers Set 1	R2
777 713		R3
777 714		R4
777 715		R5
777 716	Supervisor	R6(SP)
777 717	User	R6 (SP)
777 740	Low Error Address (PDP-11/70)	
777 742	High Error Address (PDP-11/70)	
777 744	Memory System Error (PDP-11/70)	
777 746	Cache Control	
777 750	Maintenance	
777 752	Hit/Miss	
777 754		
777 756		
777 760	Lower Size	System Size (PDP-11/70)
777 762	Upper Size	
777 764	System I/D	(PDP-11/70)
777 766	CPU Error	(PDP-11/70)
777 770	Microprogram Break (PDP-11/70)	
777 772	Program Interrupt Request (PIR)	
777 774	Stack Limit (SL) (PDP-11/70)	
777 776	Processor Status Word (PS)	

**NOTE:** All presently unused UNIBUS addresses are reserved by Digital.



**EXPANSION BOXES**

	<b>BA11-KE (KF)</b>	<b>BA11-KW (KX)</b>	<b>BA11-LE (LF)</b>
<b>MOUNTING CODE</b>	10.5 in (26.7 cm) PANEL SPACE	10.5 in (26.7 cm) PANEL SPACE	5.25 in (13.3 cm) PANEL SPACE
<b>MOUNTING SPACE PROVIDED</b>	5 SYSTEM UNITS	5 SYSTEM UNITS	2 SYSTEM UNITS
<b>CURRENT DRAWN</b>	12 A @ 120 Vac	12 A @ 120 Vac	5 A @ 120 Vac
<b>CURRENT AVAILABLE</b>	50 A @ + 5 Vdc 4 A @ + 15 Vdc 10 A @ - 15 Vdc	50 A @ + 5 Vdc 4 A @ + 15 Vdc 10 A @ - 15 Vdc	32 A @ + 5 Vdc 2 A @ + 15 Vdc 2 A @ - 15 Vdc
<b>REQUIRED CABINETS SYSTEMS</b>	H960 SERIES	H9640 SERIES H9600 SERIES	PDP-11/24, PDP-11/34A, & PDP-11/44 SYSTEMS
<b>CABLE INCLUDED</b>	BC11A	BC11A	BC11A



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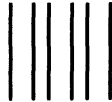
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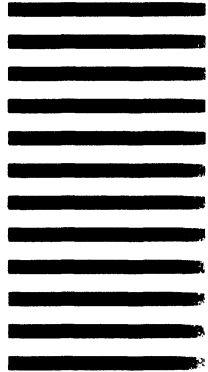
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